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DECLARATION OF ACCURACY OF TRANSLATION
IN LIEU OF SWORN TRANSLATION (37 C.F.R. 1.68)

The undersigned translator, having an office at

c/o TAKAHASHI & KITAYAMA
4th Fl., Tohsei Building,
3-12-1 Taito, Taito-ku, Tokyo 110-0016 Japan

certifies and declares that:

(1) I am fully conversant both with the Japanese and English languages.

(2) I have translated into English Japanese Patent Application Number Hei 8-189424 filed in Japan on July 18, 1996. A copy of said English translation is attached hereto.

(3) The translation is, to the best of my knowledge and belief, an accurate translation from the Japanese into the English language.

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001, of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the matter with which this translation is used.

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Keishiro Takahashi
Dr. Keishiro TAKAHASHI

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[INVENTOR]	
[Address or Domicile]	c/o FUJITSU LIMITED 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa
[Name]	Shinichiroh IKEMASU
[INVENTOR]	
[Address or Domicile]	c/o FUJITSU LIMITED 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa
[Name]	Narumi OKAWA
[APPLICANT]	
[Discrimination No.]	000005223
[Name or Appellation]	FUJITSU LIMITED
[Representative]	Tadashi SEKIZAWA
[ATTORNEY]	
[Discrimination No.]	100072590
[Attorney]	
[Name]	Sadakazu IGETA
[Telephone No.]	044-754-3035
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[TITLE OF THE INVENTION] SEMICONDUCTOR DEVICE AND ITS MANUFACTURE METHOD

[SCOPE OF CLAIM FOR A PATENT]

[Claim 1] A semiconductor device comprising:

a conductive pattern including at least one layer of metal or metal silicide;

a first insulating film made of an insulating material other than silicon nitride, and formed on a side wall of said conductive pattern; and

a second insulating film made of silicon nitride formed to cover said first insulating film formed on an upper surface and the side wall of said conductive pattern.

[Claim 2] A semiconductor device comprising:

a conductive pattern including at least one layer of metal or metal silicide;

a first insulating film made of an insulating material other than silicon nitride and formed to cover a side wall and an upper surface of said conductive pattern; and

a second insulating film made of silicon nitride formed to cover said first insulating film covering said conductive pattern.

[Claim 3] A semiconductor device according to claim 2, wherein said first insulating film on the side wall of said conductive pattern is different from said

first insulating film on the upper surface of said conductive pattern.

[Claim 4] A semiconductor device according to claim 1 or 2, wherein said first insulating film extends under a bottom end of said second insulating film of silicon nitride positioned on the side wall of said conductive pattern.

[Claim 5] A semiconductor device according to claim 1 or 2, wherein said conductive pattern is a gate electrode of a MIS transistor.

[Claim 6] A semiconductor device according to claim 1 or 2, wherein said first insulating film is made of a silicon oxide film.

[Claim 7] A semiconductor device according to claim 2, wherein said first insulating film is thicker at the upper surface of said conductive pattern than at the side wall thereof.

[Claim 8] A semiconductor device according to any one of claims 1 to 5, further comprising:

a third insulating film having etching characteristics different from a silicon nitride film and formed on said second insulating film made of a silicon nitride film; and

a contact window formed in said third insulating film and having a bottom portion at least partially defined by said second insulating film.

[Claim 9] A semiconductor device according to claim 8, wherein the surface of said third insulating

film is generally parallel to the semiconductor substrate.

[Claim 10] A semiconductor device comprising:

a plurality of first conductive layers disposed on a substrate generally in parallel;

a first insulating film formed on said first conductive layers;

a second insulating film made of a silicon nitride film and formed on said first insulating film;

a first contact window formed in and through said first and second insulating films between said plurality of first conductive layers;

a second conductive layer formed in said first contact window;

a third insulating film having etching characteristics different from a silicon nitride film and formed on said second insulating film made of the silicon nitride film;

a second contact window formed in said third insulating film at the position over said second conductive layer; and

a third conductive layer connected to said second conductive layer via said second contact window.

[Claim 11] A semiconductor device according to claim 10, wherein said second contact window extends to an area over said second insulating film formed at the outside of said second conductive layer.

[Claim 12] A semiconductor device according to

claim 10, further comprising a fourth insulating film made of a silicon nitride film, formed on said third conductive film, and having a thickness larger than that of said second insulating film.

[Claim 13] A semiconductor device comprising:

a gate electrode of a MIS transistor formed on a gate insulating film on a semiconductor substrate;

first and second impurity diffusion regions constituting source and drain of the MIS transistor formed in the semiconductor substrate on both sides of said gate electrode;

a first insulating film formed on the semiconductor substrate inclusive of said gate electrode and said first and second impurity diffusion regions;

a second insulating film of a silicon nitride film formed on said first insulating film;

a first contact window formed in and through said first and second insulating films and reaching said first impurity diffusion region;

a second contact window reaching said second impurity diffusion region;

a second conductive layer formed in said first contact window and connected to said first impurity diffusion region;

a third conductive layer formed in said second contact window and connected to said second impurity diffusion region;

a third insulating film formed on said second

insulating film inclusive of said second and third conductive layers;

a third contact window formed through said third insulating film and reaching said second conductive layer; and

a fourth conductive layer connected to said second conductive layer via said third contact window.

[Claim 14] A semiconductor device according to claim 13, further comprising:

a fourth contact window formed through said third insulating film and reaching said third conductive layer connected to said second impurity diffusion region;

a fifth conductive layer constituting a storage electrode connected to said third conductive layer via said fourth contact window; and

a sixth conductive layer constituting an opposing electrode formed to face said fifth conductive layer, with a capacitor insulating film being interposed between said fifth and sixth conductive layers.

[Claim 15] A semiconductor device according to claim 14, wherein said fifth conductive layer has a bottom portion and a cylindrical portion vertical to said semiconductor substrate.

[Claim 16] A semiconductor device according to claim 13, wherein said third contact window extends to an area over said second insulating film formed at the outside of said second conductive layer.

[Claim 17] A semiconductor device according to

claim 14, wherein said fourth contact window extends to an area over said second insulating film formed at the outside of said third conductive layer.

[Claim 18] A semiconductor device according to claim 14, wherein part of the bottom portion of said fifth conductive layer is in contact with an upper portion of said second insulating film.

[Claim 19] A semiconductor device according to claim 14, wherein the end portion of said sixth conductive layer and the end portion of said second insulating film are registered in a plan view.

[Claim 20] A semiconductor device according to claim 13, wherein said fourth conductive layer is a lamination of a conductive member and a fourth insulating film made of a silicon nitride film, and the fourth insulating film is thicker than said second insulating film.

[Claim 21] A semiconductor device comprising:

a gate electrode of a MIS transistor formed on a gate insulating film on a silicon substrate;

impurity diffusion regions constituting a source and a drain of the MIS transistor formed in the semiconductor substrate on both sides of said gate electrode;

a first insulating film formed on said semiconductor substrate inclusive of said gate electrode and said impurity diffusion regions;

a first contact window formed through said first

insulating film and reaching at least one of said impurity diffusion regions;

a second conductive layer formed in said first contact window and connected to one of said impurity diffusion regions;

a second insulating film formed on said first insulating film inclusive of said second conductive layer;

a third insulating film of a silicon nitride film formed on said second insulating film;

a second contact window formed in and through said second and third insulating films and connected to said impurity diffusion regions;

a third conductive layer constituting a storage electrode connected to said second conductive layer via said second contact window, said third conductive layer having a bottom portion and a cylindrical portion vertical to said semiconductor substrate; and

a fourth conductive layer facing said third conductive layer with a capacitor insulating film being interposed therebetween, part of said fourth conductive layer being in contact with the surface of said third insulating film via the capacitor insulating film.

[Claim 22] A semiconductor device according to claim 21, wherein the end portion of said fourth conductive layer and the end portion of said third insulating film are registered in a plan view.

[Claim 23] A semiconductor device comprising:

first and second conductive layers formed at levels different in distance from the substrate surface, the levels becoming higher in the order of the first and second conductive layers;

a first insulating film formed on said substrate, covering said first and second conductive layers;

a first contact window formed through said first insulating film and exposing the top surface of said first conductive layer;

a second contact window formed in and through said first insulating film and said second conductive layer, said second conductive layer having a side wall exposed in said second contact window; and

a pair of third conductive layers formed at least in said first and second contact windows and connected via said first contact window to the surface of said first conduction layer and to the side wall of said second conductive layer via said second contact window,

wherein D1 is larger than D2, where D1 is a depth from the surface of said first insulating film to said first conductive layer and D2 is a depth from the surface of said first insulating film to said second conductive layer.

[Claim 24] A semiconductor device according to claim 23, further comprising a second insulating film formed under said second conductive layer and having etching characteristics different from said first insulating film.

[Claim 25] A semiconductor device according to claim 234, wherein said second contact window is formed through said first insulating film, said second conductive layer, and said second insulating film.

[Claim 26] A semiconductor device according to claim 24 or 25, wherein said second insulating film is a silicon nitride film.

[Claim 27] A semiconductor device comprising:

first to third conductive layers formed at levels different in distance from a substrate surface;

a first insulating film formed on the substrate inclusive of said first to third conductive layers;

a second insulating film formed under said second conductive layer and having etching characteristic different from said first insulating film;

a third insulating film formed on said third conductive layer and having etching characteristics same as said second insulating film;

a first contact window formed through said first insulating film and exposing the top surface of said first conductive layer;

a second contact window formed through said first insulating film, said second conductive layer, and said second insulating film;

a third contact window formed through said first and third insulating films and exposing the surface of said third conductive layer; and

fourth conductive layers respectively connected to

the surface of said first conductive layer via said first contact window, to the side wall of said second conductive layer via said second contact window, and to the surface of said third conductive layer via said third contact window,

wherein D1 > D3 > D2, where D1 is a depth from the surface of said first insulating film to said first conductive layer, D2 is a depth from the surface of said first insulating film to said second conductive layer, and D3 is a depth from the surface of said first insulating film to said third conductive layer.

[Claim 28] A semiconductor device according to claim 27, wherein said second and third insulating films are made of a silicon nitride film.

[Claim 29] A semiconductor device according to claim 23 or 27, wherein the surface of said first insulating film is planarized to be generally parallel to said substrate.

[Claim 30] A semiconductor device according to claim 23 or 27, wherein said second conductive layer is a capacitor opposing electrode of a capacitor.

[Claim 31] A semiconductor device comprising:

a plurality of first conductive layers formed on the surface of a semiconductor substrate generally in parallel;

first insulating films formed to cover said first conductive layers;

a second insulating film embedded between adjacent

ones of said first conductive layers, said second insulating film having a surface coincident with the upper surface of said first insulating films and parallel to the surface of the semiconductor substrate; and

a contact window formed in said second insulating film, part of said contact window riding upon one of said first insulating films.

[Claim 32] A semiconductor device comprising:

a plurality of first conductive layers formed on the surface of a semiconductor substrate generally in parallel and having a plurality of levels different in distance from the surface of the semiconductor substrate;

first insulating films formed to cover said first conductive layers; and

a second insulating film embedded between adjacent ones of said first conductive layers and having a surface coincident with the upper surface of said first insulating films with the highest level in distance from the surface of said first insulating film and parallel to the surface of said semiconductor substrate.

[Claim 33] A semiconductor device according to claim 32, further comprising a contact window formed in said second insulating film, part of said contact window extending to an area over one of said first insulating films.

[Claim 34] A semiconductor device according to

claim 31 or 32, wherein said first insulating films are each made of a silicon nitride film.

[Claim 35] A semiconductor device according to claim 31, wherein said first conductive layers with the highest level in distance from the surface of the semiconductor substrate are formed on a field insulating film, and said first conductive layers with the lowest level in distance from the surface of said semiconductor substrate are formed on the active regions.

[Claim 36] A semiconductor device according to claim 31, wherein said first conductive layer is a DRAM bit line.

[Claim 37] A semiconductor device according to claim 32, wherein said first conductive layer is a DRAM word line.

[Claim 38] A semiconductor device comprising:

a gate electrode of a MIS transistor formed on a gate insulating film on a silicon substrate;

first and second impurity diffusion regions constituting source and drain of the MIS transistor formed in said silicon substrate on both sides of the gate electrode;

an insulating film formed on the silicon substrate inclusive of said gate electrode and said first and second impurity diffusion regions;

a pair of contact windows formed in and through said insulating film and reaching said first and second impurity diffusion regions;

first and second conductive layers made of the same conductive layer and connected to said first and second impurity diffusion regions via said contact windows;

a bit line connected to said first impurity diffusion area via said first conductive layer; and

a capacitor storage electrode connected to said second impurity diffusion region via said second conductive layer,

wherein the impurity concentration of said second impurity diffusion region is larger than the impurity concentration of said first impurity diffusion region.

[Claim 39] A semiconductor device comprising:

a gate electrode of a MIS transistor formed on a said gate insulating film on a silicon substrate;

first and second impurity diffusion regions constituting source and drain of the MIS transistor, having the same impurity concentration and formed in the silicon substrate on both sides of the gate electrode;

an insulating film formed on said silicon substrate inclusive of said gate electrode and said first and second impurity diffusion regions;

a pair of contact windows formed through said insulating film and reaching said first and second impurity diffusion regions;

a third impurity diffusion region of the same conductivity type as said second impurity diffusion region formed in said silicon substrate under said

contact window merging with said second impurity diffusion region, the impurity concentration of said third impurity diffusion region being larger than the impurity concentrations of said first and second impurity diffusion regions;

a first conductive layer connected to said first impurity diffusion area via one of said contact windows;

a second conductivity layer made of the same conductive layer as said first conductive layer and connected to said second impurity diffusion region and said third impurity diffusion region via the other of said contact windows;

a bit line connected to said first impurity diffusion region via said first conductive layer; and

a capacitor storage electrode connected to said second impurity diffusion region via said second conductive layer,

wherein the impurity concentration of said third impurity diffusion region is larger than the impurity concentration of said first and second impurity diffusion regions.

[Claim 40] A method of manufacturing a semiconductor device comprising the steps of:

forming a conductive layer including at least one layer of metal silicide on a semiconductor substrate;

depositing a first silicon nitride film on the conductive layer;

patterning a lamination of the conductive layer

and the first silicon nitride;

forming an oxide film on a side wall of the conductive layer by thermal oxidation;

forming a second silicon nitride film on the semiconductor substrate including the patterned lamination and the oxide film on the side wall; and

anisotropically etching the second silicon nitride film to form a side wall spacer of the second silicon nitride on the side wall of the lamination inclusive of the oxide film on the side wall.

[Claim 41] A method of manufacturing a semiconductor device comprising the steps of:

forming a conductive layer including at least one layer of metal silicide on a semiconductor substrate;

sequentially forming a first insulating film and a first silicon nitride film on the conductive layer;

patterning a lamination of the conductive layer, the first insulating film and the first silicon nitride;

forming an oxide film on a side wall of the conductive layer by thermal oxidation;

forming a second silicon nitride film on the semiconductor substrate including the patterned lamination and the oxide film on the side wall; and

anisotropically etching the second silicon nitride film to form a side wall spacer of the second silicon nitride on the side wall of the lamination inclusive of the oxide film on the side wall.

[Claim 42] A method according to claim 41,

wherein the first insulating film is thicker than the oxide film.

[Claim 43] A method according to claim 40 or 41, further comprising a step of forming a second insulating film and a step of forming a contact window through the second insulating film, part of the bottom of the contact window rides at least upon part of the second silicon nitride.

[Claim 44] A method according to claim 43, further comprising a planarizing step to be performed after the second insulating film is formed.

[Claim 45] A method according to claim 41, wherein the first insulating film is formed by thermal oxidation or vapor phase growth.

[Claim 46] A method according to claim 41, wherein the first insulating film is a lamination film formed by thermal oxidation and vapor phase growth.

[Claim 47] A manufacture method comprising the steps of:

forming a gate insulating film and a first conductive layer on a semiconductor substrate and patterning the first conductive layer to form gate electrodes of MIS transistors;

forming impurity diffusion regions constituting source and drain regions in the semiconductor substrate by using the gate electrodes as a mask;

forming a first insulating film on the semiconductor substrate inclusive of said gate

electrodes;

forming a second insulating film made of a silicon nitride film on the first insulating film;

selectively and sequentially etching the second and first insulating films to form first contact windows reaching at least ones of the impurity diffusion regions;

forming second conductive layers in the first contact windows;

forming a third insulating film on the second insulating film inclusive of the second conductive layers;

forming second contact windows through the third insulating film, the second contact windows being connected to the second conductive layers; and

forming third conductive layers connected to the second conductive layers via the second contact windows.

[Claim 48] A method according to claim 47, further comprising a step of forming the third conductive layer as a lamination of a conductive layer and a silicon nitride film, the silicon nitride film being thicker than the second insulating film.

[Claim 49] A method according to claim 47 further comprising the steps of:

forming a fourth insulating film on the whole surface of the substrate;

forming a third contact window reaching the second conductive layer, by selectively removing the fourth and

third insulating films on the second conductive layer where the third conductive layer is not formed;

selectively forming a fourth conductive layer on the bottom and side wall surfaces of the third contact window;

removing the fourth insulating film by using the fourth conductive layer as a mask and the second insulating film as an etching stopper to expose the fourth conductive layer in a cylindrical shape;

forming a fifth insulating film on the surface of the fourth conductive layer;

forming a fifth conductive layer on the semiconductor substrate inclusive of the fifth insulating film; and

selectively removing the fifth conductive layer by leaving at least part of the fifth conductive layer inclusive of the fourth conductive layer.

[Claim 50] A method according to claim 49, further comprising the steps of:

forming a sixth insulating film of a silicon nitride film covering the upper surface and side wall of the third conductive layer; and

removing the fourth insulating film by using the second and sixth insulating films as an etching stopper.

[Claim 51] A method according to claim 49, wherein said step of selectively removing the fifth conductive layer includes a step of removing the fifth conductive layer and the fifth and second insulating

films by using the same mask.

[Claim 52] A method of manufacturing a semiconductor device comprising the steps of:

sequentially forming on a semiconductor substrate a first conductive layer, a first insulating film, a second insulating film made of silicon nitride, and a third insulating film;

forming a contact window reaching said first conductive layer by sequentially etching the third, second, and first insulating films;

selectively forming a second conductive film on the bottom and side wall of the contact window;

removing said third insulating film by using the second conductive layer as a mask and the second insulating film as an etching stopper to expose the second conductive layer of cylindrical shape;

forming a fourth insulating film on the surface of the second conductive film;

forming a third conductive layer on the semiconductor substrate inclusive of the fourth insulating film; and

selectively removing the third conductive layer leaving at least part of an area inclusive of the second conductive layer.

[Claim 53] A method according to claim 52, wherein said step of selectively removing the third conductive layer includes a step of removing the third conductive layer and the fourth and second insulating

films by using the same mask.

[Claim 54] A manufacture method comprising the steps of:

forming a gate insulating film and a first conductive layer on a semiconductor substrate, and patterning said first conductive layer to form a gate electrode of a MIS transistor;

forming impurity diffusion regions constituting a source and a drain in the semiconductor substrate by using the gate electrode as a mask;

forming a first insulating film on the semiconductor substrate inclusive of the gate electrode;

selectively etching said first insulating film to form first contact windows reaching the impurity diffusion regions;

forming second conductive layers in the first contact windows;

forming a second insulating film on the first insulating film inclusive of the second conductive layers;

forming a second contact window through the second insulating film to expose one of the second conductive layers;

forming a third conductive layer connected to one of the second conductive layers via the second contact window;

sequentially forming on the semiconductor substrate inclusive of the third conductive layer a

third insulating film, a fourth insulating film made of silicon nitride, and a fifth insulating film;

selectively removing the fifth, fourth, third, and second insulating films over the other of the second conductive layer where the third conductive layer is not formed, to form a third contact window reaching the other of the second conductive layer;

selectively forming a fourth conductive layer on the bottom and side wall of the third contact window;

removing the fifth insulating film by using the fourth conductive layer as a mask and the fourth insulating film as an etching stopper to expose the fourth conductive layer of cylindrical shape;

forming a sixth insulating film on the surface of the fourth conductive layer;

forming a fifth conductive layer on the semiconductor substrate inclusive of the sixth insulating film; and

selectively removing the fifth conductive layer leaving at least part of an area inclusive of the fourth conductive layer.

[Claim 55] A method according to claim 54, further comprising the steps of:

forming a capacitor by using the fourth conductive layer as a storage electrode, the fifth conductive layer as an opposing electrode, and the sixth insulating film as a capacitor dielectric film;

forming a seventh insulating film on the

semiconductor substrate inclusive of the memory cell area and the other peripheral area; and

planarizing the seventh insulating film so as make the memory cell area flush with the peripheral area.

[Claim 56] A method according to claim 55 wherein said step of selectively removing the fifth conductive layer includes a step of removing the fifth conductive layer and the sixth and fourth insulating films by using the same mask.

[Claim 57] A method of manufacturing a semiconductor device comprising the steps of:

forming first conductive layers on a semiconductor substrate;

forming a first insulating film on the first conductive layers;

forming second conductive layers on the first insulating film;

forming a second insulating film on the semiconductor substrate inclusive of the second conductive layers;

forming a mask on the second insulating film for forming contact windows; and

sequentially etching the second and first insulating films by using the mask to form a contact window over the first conductive layer and sequentially etching the second insulating film and second conductive layer by using the mask to form a contact window through the second conductive layer.

[Claim 58] A method according to claim 57, further comprising a step of generally planarizing the surface of the second insulating film.

[Claim 59] A method of manufacturing a semiconductor device comprising the steps of:

forming first conductive layers on a semiconductor substrate;

sequentially forming a first insulating film and a second insulating film made of a silicon nitride film on the first conductive layers;

forming a second conductive layer on the second insulating film;

selectively removing the second insulating film at least at an area of a contact portion of one of the first conductive layers;

forming a third insulating film on the semiconductor substrate inclusive of the second insulating film, the first insulating film, and the semiconductor substrate;

forming a mask on the third insulating film for forming contact windows; and

sequentially etching the third and first insulating films by using the mask to form a contact window over the first conductive layer and sequentially etching the third insulating film and second conductive layer by using the mask to form a contact window penetrating through the second conductive layer.

[Claim 60] A method according to claim 59,

further comprising a step of generally planarizing the third insulating film.

[Claim 61] A method of manufacturing a semiconductor device comprising:

forming first conductive layers on a semiconductor substrate;

forming a first insulating film on the first conductive layers;

forming a lamination of a second conductive layer and a second insulating film made of a silicon nitride film stacked on the second conductive layer, on the first insulating film;

forming a third insulating film and a fourth insulating film made of a silicon nitride film, on the semiconductor substrate inclusive of the lamination and the first insulating film;

forming a third conductive layer on the fourth insulating film;

selectively removing the fourth insulating film at least at an area of a contact portion of one of the first and second conductive layers;

forming a fifth insulating film on the semiconductor substrate inclusive of the fourth and third insulating films and the third conductive layer;

forming a mask on the fifth insulating film for forming contact windows; and

sequentially etching the fifth, third, and first insulating films by using the mask to form a contact

window over one of the first conductive layers, sequentially etching the fifth, third, and second insulating films by using the mask to form a contact window over the second conductive layer, and sequentially etching the fifth insulating film, the third conductive layer, and the fourth insulating film by using the mask to form a contact window through the second conductive layer.

[Claim 62] A method according to claim 61, further comprising a step of generally planarizing the fifth insulating film.

[Claim 63] A method of manufacturing a semiconductor device comprising the steps of:

sequentially forming a first conductive layer and a first insulating film on a semiconductor substrate;

patterning a lamination of the first insulating film and the first conductive layer into lamination units disposed generally parallel;

forming a second insulating film on the semiconductor substrate inclusive of the lamination units and anisotropically etching the lamination units to form side spacers on side walls of the lamination units;

forming a third insulating film on the semiconductor substrate inclusive of the first conductive layer covered with the first and second insulating films;

planarizing the third insulating film by CMP by

using the first insulating film as a stopper; and

partially removing the third insulating film to form a contact window, part of the bottom of the contact window extending at least over part of the second insulating film.

[Claim 64] A method of manufacturing a semiconductor device comprising the steps of:

forming an element isolating insulating film on a semiconductor substrate to define an active region;

sequentially forming a first conductive layer and a first insulating layer on the semiconductor substrate inclusive of the element isolating insulating film and the active region;

patterning a lamination of the first insulating film and the first conductive layer into lamination units disposed generally parallel;

forming a second insulating film on the semiconductor substrate inclusive of the lamination units and anisotropically etching the lamination units to form side spacers on side walls of the lamination units;

forming a third insulating film on the semiconductor substrate inclusive of the first conductive layer covered with the first and second insulating films and the element isolating insulating film; and

planarizing the third insulating film by CMP by using the first insulating film on the element

separation insulating film as a stopper.

[Claim 65] A method according to claim 64, wherein part of the third insulating film on the active region is removed to form a contact window whose part of the bottom rides on part of the second insulating film.

[Claim 66] A method according to claim 63 or 64, wherein the first and second insulating films are silicon nitride films.

[Claim 67] A method of manufacturing a semiconductor device comprising the steps of:

forming a gate oxide film and a gate electrode on a semiconductor substrate of a first conductivity type;

implanting first impurity ions of a second conductivity type opposite to the first conductivity type into the semiconductor substrate by using the gate electrode as a mask to form first and second impurity diffusion regions constituting source/drain regions;

forming an insulating film on the semiconductor substrate covering the gate electrode;

partially etching the insulating film to form a first contact window reaching the first impurity diffusion region and a second contact window reaching the second impurity diffusion region;

covering the second contact window with a mask pattern;

implanting second impurity ions of the second conductivity type into the first impurity diffusion region exposed in the first contact window by using the

mask pattern and the insulating film as a mask to form a third impurity diffusion region;

forming a first conductive layer connected to the third and first impurity diffusion regions via the first contact window and a second conductive layer connected to the second impurity diffusion region via the second contact window;

forming a DRAM storage electrode connected to the third and first impurity diffusion regions via the first conductive layer; and

forming a DRAM bit line connected to the second impurity diffusion regions via the second conductive layer.

[Claim 68] A method according to claim 67, wherein the mask pattern is made of resist.

[Claim 69] A method according to claim 67, wherein a dose of second conductivity ion implantation is larger than a dose of first conductivity ion implantation.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Industrial Field of Utilization]

The present invention relates to a semiconductor memory device and its manufacture, and more particularly to a semiconductor memory device and its manufacture suitable for highly integrated and reliable DRAMs (Dynamic Random Access Memories).

[0002]

[Prior Art]

As the capacity of DRAM becomes large, it becomes essential to make its fundamental constituent, a memory cell, more finer in order to realize high integration and low cost.

A general DRAM cell is constituted of one MOS transistor and one capacitor. In order to make a memory cell finer, it is therefore substantial that how a large capacitance is obtained from a small cell size.

[0003]

As a method of procuring a capacitance of a memory cell, a trench type cell and a stack type cell have recently been proposed and adopted the cell structure of current DRAMs. A trench type cell has a capacitor formed in a trench in the substrate. A stack type cell has a capacitor three-dimensionally stacked above the MOS transistor.

More improved cell structures have also been proposed, particularly for stack type cells, such as a fin type cell and a cylinder type cell. A fin type cell has a plurality of storage electrodes disposed generally in parallel with the substrate and the upper and lower surfaces of each storage electrode are used as capacitor electrodes so that the capacitance per unit area occupied by a cell can be increased more than a stack type cell. A cylinder type cell has a cylindrical storage electrode disposed generally vertically to the substrate to increase the capacitance.

[0004]

By using these cell structures and their manufacture processes, it becomes possible to realize DRAMs of 64 Mbit class with 0.35 μm design rule.

[0005]

[Problems that the Invention is to solve]

However, these technologies only are insufficient for higher integration such as DRAMs of 256 Mbit and 1 Gbit class with 0.25 μm to 0.15 μm design rule.

It is therefore necessary not only to reduce a substrate area occupied by a capacitor but to make as small as possible an alignment margin set for eliminating troubles to be caused by wiring shortages or the like during photolithography. It is also necessary to solve the problems associated with improved cell structures such as a cylinder type cell.

[0006]

A first problem pertains to alignment.

A self align contact (SAC) method is already known as a method of forming a fine contact window. This method is disclosed, for example, in Japanese Patent Laid-open Publication No. 58-115859. With this method, a first insulating film is formed on a gate electrode layer of a MOS transistor and patterned to form a gate electrode.

[0007]

After source/drain diffusion regions are formed, a second insulating film is formed and etched through

anisotropic etching until the diffusion regions are exposed. Since an insulating film is formed on the side wall of a gate electrode portion including the first insulating film, the periphery of the gate electrode can be perfectly insulated with the first and second insulating films. Contact window areas can also be formed above the diffusion regions in a self alignment manner.

[0008]

If the self align method is used for forming contact windows as described above, an alignment margin is not necessary between the underlying conductive layers and contact windows. The cell can be made fine correspondingly because the alignment margin is not necessary. Such a simple self align method is still unsatisfactory because multi-layer processes are used for making highly integrated DRAM cells finer.

[0009]

An example of improved self align contact techniques used for DRAM cells will be described with reference to schematic cross sectional views of Fig. 34 to 35 which illustrate manufacture processes.

Figs. 34 and 35 are cross sectional views of typical memory cell units taken along the direction crossing the word line direction. With reference to these drawings, a method of forming contact windows by using the self-align contact technique will be described specifically, the contact windows being used for contact

between each of bit lines and storage electrode with the source/drain diffusion region of the MOS transistor.

[0010]

First, as shown in Fig. 34(a), a gate insulating film 113 is formed on a silicon substrate 111 surrounded by a LOCOS oxide film 112. On this gate insulating film 113, a polysilicon layer 114 and a tungsten silicide layer 115 are deposited to form a polycide gate electrode. Source/drain regions 116 are formed on both sides of the gate electrode. A nitride film 117 is formed surrounding the periphery of the polycide gate electrode which corresponds to the word line.

[0011]

The processes up to this are the same as the above-described self align contact method so that these processes can be executed in accordance with the method described in the Japanese Patent Laid-open Publication No. 58-115859.

Next, a silicon oxide film 118 is formed over the whole surface of the nitride film 117. The silicon oxide film 118 is planarized by chemical mechanical polishing (CMP) or the like to facilitate the succeeding processes.

[0012]

Next, as shown in Fig. 34(b), on the planarized oxide film 118, a resist layer is coated and patterned by usual photolithography to form a resist pattern 119 to be used as an etching mask.

Next, as shown in Fig. 35(a), by using the resist pattern 119 as a mask, the oxide film 118 is etched to form contact windows 120 reaching the diffusion regions 116. In this case, the etching conditions of the oxide film is set so as to have a large etching selection ratio of the oxide film to the silicon nitride film. Therefore, even if the nitride film 117 is exposed while etching the oxide film, the nitride film is not etched so much and the areas generally the same as those of the self align contact windows first formed in the nitride film become new contact windows.

[0013]

Next, the resist pattern 119 is removed by known techniques.

Then, as shown in Fig. 35(b), a conductive layer 121 is formed on the contact windows.

With the above method, even if the contact windows are formed above or near the gate electrode because of displacement of the resist pattern 119, the conductive layer 121 and polycide electrode are not electrically short-circuited. Therefore, it is not necessary to have an alignment margin of the contact window relative to the polycide electrode.

[0014]

According to this technique, contact windows can be formed in a self alignment manner, while planarizing the oxide film 118 serving as an interlayer insulating film.

Such self align contact technique will be called hereinafter "nitride film spacer SAC".

The following problems occur when nitride spacer SAC is used.

[0015]

One problem associated with the gate electrode structure formed by nitride film spacer SAC is the deteriorated transistor characteristics.

The problems of the gate electrode structure using a nitride film spacer side wall are described, for example, in IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 38, NO. 3 MARCH 1991 "Hot-Carrier Injection Suppression Due to the Nitride-Oxide LDD Spacer Structure", T. Mizumo et. al.

[0016]

This paper describes that as compared to a MOS transistor with an oxide film side wall, the electrical characteristics of a MOS transistor with a nitride film side wall are deteriorated greatly, for example, in the hot carrier effects, leading to a lower reliability. This may be ascribed to a larger number of traps in a silicon nitride film than in an oxide film.

[0017]

The above paper discloses a method of preventing deterioration of transistor characteristics by forming an oxide film between the nitride film side wall and gate electrode and between the nitride film side wall and substrate so as to suppress the influence of the

nitride film.

However, such a structure cannot be applied directly to the nitride film spacer SAC structure.

[0018]

This problem will be explained with reference to Figs. 36 and 37. Similar to Figs. 34 and 35, cross sectional views of typical memory cell units shown in Figs. 36 and 37 are taken along the direction crossing the word line direction. In Figs. 36 and 37, similar elements to those shown in Figs. 34 and 35 are represented by using identical reference numerals.

Fig. 36(a) illustrates the processes corresponding to those of Fig. 34(b), and shows a resist pattern 118 on an oxide film 117, which pattern is used for forming contact windows. A silicon nitride film 122 is formed on a polycide electrode constituted of a silicon film 114 and a silicide film 115, and a silicon nitride film 124 is formed via an oxide film 123 on the side wall of the laminated structure of the polycide electrode and silicon nitride film 122. Impurity doped regions 116 as source/drain diffused regions are formed in the substrate 111 on both sides of the gate electrode.

[0019]

The resist pattern 118 is formed in order to form contact windows of the nitride film spacer SAC structure. In Fig. 36(a), the resist pattern 119 is displaced because of misalignment.

If the oxide film 117 is etched in this state, the

side wall oxide film 123 between the nitride film side wall 124 and polycide electrode is also etched at the same time, and the side wall of the gate electrode is exposed, as shown in Fig. 36(b).

[0020]

Next, as a wiring electrode 121 is formed in the contact window, as shown in Fig. 37 the gate electrode is electrically shorted to the wiring electrode 121 and diffusion regions 116 via the side wall of the exposed gate electrode.

In order to avoid such electrical short circuits, it is necessary to have an alignment margin and it is impossible to form contact windows in a self alignment manner. The nitride film side wall structure descried in the above paper cannot be therefore applied to nitride film spacer SAC.

[0021]

Another problem associated with nitride film spacer SAC is separation or peel-off of a silicide film to be caused by a combination of a polycide conductive layer and nitride film spacer SAC.

A polycide structure, which is a lamination structure of a silicon film and a silicide film such as tungsten silicide (WSi) and molybdenum silicide (MoSi), has a resistance lower than a silicon film and is widely used for gate electrodes, word lines, bit lines, and the like.

[0022]

It has been found, however, that if the nitride film spacer SAC process is used with a polycide conductive film, stress is generated because of a difference of thermal expansion coefficient between the polycide film and nitride film and the silicide film can be separated at later heat treatments.

The conventional nitride film spacer SAC cannot be used therefore also for the wiring structure of bit lines or the like, which do not deteriorate transistor performances.

[0023]

According to a first aspect of the present invention, the above problems are solved by providing a method of realizing fine and highly integrated DRAM memory cells by making it possible to apply the nitride film spacer SAC structure to the polycide structure.

A second problem is associated with a process of forming a contact hole to expose a plug conductive film embedded in another contact window.

[0024]

For highly integrated DRAM structures, a planarizing process is necessary for preventing breakage or the like of a wiring layer at later processes. For this reason, a structure is adopted which embeds a conductive film called a plug into a contact window.

A process of forming a contact window for contacting a plug with an upper wiring layer is desired to have a process margin relative to the position

misalignment. It is also preferable to use SAC in forming a contact window because fine processing is possible.

[0025]

Under the conditions that an insulating film surrounding a plug can be etched by the contact window forming process, it is not possible to have a process margin relative to the position misalignment and to use SAC. Therefore, a position alignment margin becomes necessary, which hinders high integration.

According to a second aspect of the invention, the above problems are solved by providing means for enabling the application of the SAC structure with some process margin for the position misalignment on the plug.

[0026]

A third problem is associated with a method of forming a cylinder type storage electrode.

A cylinder type storage electrode utilizes the side wall portion of the cylinder as part of the capacitor of a memory cell. It is therefore necessary to make constant the side wall area of the cylinder in order to stabilize the capacitance.

Generally a cylinder type storage electrode is formed by forming an opening in an insulating film, leaving a conductive layer as the storage electrode only on the side wall and bottom of the opening, and thereafter etching and removing the insulating film.

[0027]

With these processes, the exposed area of the outer side wall of a cylinder type conductive layer used as the storage electrode changes with an amount of etching the insulating film on the outer side wall of the storage electrode.

According to a third aspect of the invention, the above problems are solved by providing a method of obtaining a stable capacitance by making constant the exposed area of an outer side wall of a cylinder type storage electrode.

[0028]

A fourth problem is associated with a process of forming a contact window for a conductive layer having a large step.

The structure capable of increasing the area of a storage electrode by using a three-dimensional structure such as a cylinder type cell described above has been studied in order to procure a sufficient capacitance even with a small cell area. A height of the storage electrode is required to be made greater in order to procure a sufficient capacitance. Therefore, a height difference (step) between a cell area and a peripheral circuit area becomes large.

[0029]

Such a step poses not only a problem of breakage of wiring at the step, but also another problem. Namely, a size accuracy is lowered when wirings over the cell area and peripheral circuit area are patterned, because

of an insufficient depth of focus.

There is a method of solving these problems, as disclosed in Japanese Patent Laid-open Publication No. 3-155663, which embeds concave areas on the surface of an insulating film with a coated insulating film such as spin on glass (SOG) and resist and thereafter etches it back, or planarizes the insulating film formed on uneven cell and peripheral circuit areas through chemical mechanical polishing (CMP).

[0030]

A problem of a shallow depth of focus can be solved through such planarization. However, following new problems occur.

A DRAM structure has a number of conductive layers which are connected to upper metal wiring layers, including MOS transistor source/drain diffusion regions, word lines, and bit lines respectively in a peripheral circuit area, bit lines, capacitor opposing electrodes, and the like in the memory cell area.

[0031]

These conductive layers are not formed at the same layer level, but are formed as a multi-layer structure having interlayer insulating films. Therefore, distances of conductive layers from the substrate are different.

If the higher level insulating film is planarized by the above-described processes, the surface of the insulating film is made generally parallel to the

substrate surface so that depths of contact holes formed in the insulating film become different.

[0032]

Therefore, if these contact holes are formed by a single photolithography process, until the lowermost conductive layer - diffusion region - is exposed, the uppermost conductive layer for which contact hole has already formed is exposed in an etching atmosphere for a long time.

An etching selection ratio of the insulating film to the conductive layer cannot be set too high. Therefore, the contact window for the uppermost conductive layer can penetrate into the lower insulating film. At the worst, another conductive layer under the excessively etched contact window can be electrically short-circuited.

[0033]

In order to form a highly reliable contact hole without electrical short of the lower level wiring layer, it is essential to increase the number of processes, for example, to divide the single photolithography process into a plurality of processes.

According to a fourth aspect of the present invention, there is provided means for reducing the number of manufacture processes and allowing contact holes to be opened by one photolithography process even for the structure having different depths of contact holes.

[0034]

A fifth problem is associated with planarization.

DRAM manufacture processes become complicated and the number of processes increases, as the degrees of integration and fine processing become high. These may become a factor of lowering product yields and ultimately raising the cost.

Multi-layer wiring processes are used for high integration. Planarization of insulating layers and wiring layers is therefore important.

[0035]

Planarizing technology without complicated manufacture processes is therefore desired.

According to a fifth aspect of the invention, there is provided a method of simplifying manufacture processes by applying the planarizing process to nitride film spacer SAC.

A sixth problem is associated with electrical characteristics of MOS transistors.

As integration becomes higher, MOS transistors are made finer which may cause deteriorated transistor characteristics and lowered reliability.

[0036]

According to a sixth aspect of the present invention, there is provided a MOS transistor structure with improved characteristics of MOS transistors in a DRAM memory cell area.

[0037]

[Means for Solving Problems]

According to one aspect of the present invention, the above-described problems can be solved by providing semiconductor devices characterized as in the following.

A semiconductor device comprising: a conductive pattern including at least one layer of metal or metal silicide; a first insulating film made of an insulating material other than silicon nitride formed on a side wall of the conductive pattern; and a second insulating film made of silicon nitride formed to cover the first insulating film formed on an upper surface and the side wall of the conductive pattern.

[0038]

A semiconductor device comprising: a conductive pattern including at least one layer of metal or metal silicide; a first insulating film made of an insulating material other than silicon nitride and formed to cover a side wall and an upper surface of the conductive pattern; and a second insulating film made of silicon nitride formed to cover the first insulating film covering the conductive pattern.

[0039]

In the semiconductor device, the first insulating film on the side wall of the conductive pattern is different from the first insulating film on the upper surface of the conductive pattern.

In the semiconductor device, the first insulating film extends under a bottom end of the second insulating

film of silicon nitride positioned on the side wall of the conductive pattern.

In the semiconductor device, the conductive pattern is a gate electrode of a MIS transistor.

[0040]

In the semiconductor device, the first insulating film is thicker at the upper surface of the conductive pattern than at the side wall thereof.

The above-described problems can be solved by providing semiconductor device manufacture methods characterized as in the following.

A method of manufacturing a semiconductor device comprising the steps of: forming a conductive layer including at least one layer of metal silicide on a semiconductor substrate; depositing a first silicon nitride film on the conductive layer; patterning a lamination of the conductive layer and the first silicon nitride; forming an oxide film on a side wall of the conductive layer by thermal oxidation; forming a second silicon nitride film on the semiconductor substrate including the patterned lamination and the oxide film on the side wall; and anisotropically etching the second silicon nitride film to form a side wall spacer of the second silicon nitride on the side wall of the lamination inclusive of the oxide film on the side wall.

[0041]

A method of manufacturing a semiconductor device comprising the steps of: forming a conductive layer

including at least one layer of metal silicide on a semiconductor substrate; sequentially forming a first insulating film and a first silicon nitride film on the conductive layer; patterning a lamination of the conductive layer, the first insulating film and the first silicon nitride; forming an oxide film on a side wall of the conductive layer by thermal oxidation; forming a second silicon nitride film on the semiconductor substrate including the patterned lamination and the oxide film on the side wall; and anisotropically etching the second silicon nitride film to form a side wall spacer of the second silicon nitride on the side wall of the lamination inclusive of the oxide film on the side wall.

[0042]

In the method, the first insulating film is thicker than the oxide film.

In the method, the first insulating film is formed by thermal oxidation or vapor phase growth.

In the method, the first insulating film is a lamination film formed by thermal oxidation and vapor phase growth.

[0043]

The first aspect of the invention will be described with reference to Fig. 1.

In Fig. 1(a), reference numeral 1 represents a silicon substrate, reference numeral 2 represents a field insulating film, reference numeral 3 represents a

gate oxide film, reference numeral 4 represents a silicon film, reference numeral 5 represents a silicide film, reference numeral 6 represents a silicon oxide film, reference numeral 7 represents an impurity diffused region, reference numeral 8 represents a silicon nitride film spacer, reference numeral 9 represents an interlayer insulating film, and reference numeral 10 represents a contact window.

[0044]

An active region on the substrate 1 is defined by the field insulating film 2. On the gate oxide film 3 on the active region, a gate electrode is formed which is a lamination of the silicon film 4 and silicide film 5. The silicon nitride film 8 covers the upper surface and side area of the gate electrode. The oxide film 6 is disposed under the silicon nitride film 8 serving as the side spacer and between the side wall of the gate electrode and the side spacer nitride film.

[0045]

Since the oxide film 6 is disposed under the silicon nitride film 8 serving as the side spacer, most of hot carriers generated at the MOS transistor channel are trapped in the oxide film 6. The MOS transistor characteristics are less influenced by the silicon nitride film 8. Therefore, almost the same reliability as a conventional MOS transistor using an oxide film side wall spacer can be ensured.

[0046]

Since the oxide film 6 between the side wall of the gate electrode and the nitride film functions as a relaxation film between the silicide film 5 and nitride film 8, the silicide film can be prevented from being separated from the silicon film 4 at later heat treatments or the like.

Also since the silicon oxide film 6 exists only on the side wall of the gate electrode and is not exposed on the upper surface of the gate electrode structure, the contact window 10 can be formed by using nitride film spacer SAC, without posing a problem of an electrical short circuit between a conductive layer and the gate electrode even if the mask is displaced, as described with conventional techniques.

[0047]

Fig. 1(b) shows another example of the fundamental embodiment of the invention.

In Fig. 1B, reference numeral 1 represents a silicon substrate, reference numeral 2 represents a field insulating film, reference numeral 3 represents a gate oxide film, reference numeral 4 represents a silicon film, reference numeral 5 represents a silicide film, reference numeral 7 represents an impurity diffused region, reference numeral 8 represents a silicon nitride film spacer, reference numeral 9 represents an interlayer insulating film, reference numeral 10 represents a contact window, and reference numeral 11 represents a silicon oxide film. In Fig.

1(b), elements similar to those shown in Fig. 1(a) are represented by using identical reference numerals.

[0048]

As compared to the structure shown in Fig. 1(a), the silicon oxide film is formed also on the silicide film 5 constituting the gate electrode to completely cover the upper surface and side wall of the gate electrode with the silicon oxide film 11. With this structure, since the silicon nitride film 8 and silicide film 5 do not contact directly, the structure more resistant to separation at later heat treatments or the like can be provided.

[0049]

The structures shown in Figs. 1(a) and 1(b) are applicable not only to a MOS transistor gate electrode but to other wiring layers such as bit lines having a polycide structure.

U.S. Patent No. 5,364,804 describes an oxide film formed between a polycide gate electrode and a nitride film. However, similar to the above-cited document, according to this U.S. Patent, the oxide film exists on the side wall of the nitride film on polycide. It is obvious that there is the same problem as the conventional problem described with reference to Figs. 35 and 36.

[0050]

JP-A-8-97210 describes the structure apparently similar to that shown in Fig. 1(a). However, this

publication does not describe the peel-off problem of a silicide film on which a nitride film is directly formed. It does not describe that an oxide film between the silicide film and nitride film has the effects of preventing peel-off.

[0051]

As shown in Fig. 1 of this publication, a side wall silicon oxide film is formed on the upper surface of the gate electrode. This oxide film enters the area of the silicon nitride film covering the gate electrode so that part of the silicon nitride film is thin.

With this structure, the nitride film is etched at a later process of forming a contact window, and the side wall oxide film is exposed. If this side wall oxide film is etched, there is a possibility that the gate electrode and the wiring layer formed in the contact window may be electrically shorted.

[0052]

According to the first aspect of the invention, the side wall oxide film is formed only on the side wall of the gate electrode, and the side wall oxide film does not enter the silicon nitride film covering the gate electrode. This structure is different from that described in the publication.

Since the oxide film does not enter the silicon nitride film, the silicon nitride film does not become thin. It is possible to avoid the danger that the gate electrode is exposed when the contact window is formed.

[0053]

According to this publication, in order to form the oxide film also on the side wall of the silicon nitride film on the gate electrode, the oxide film is formed by CVD. According to the present invention, the oxide film can be formed not only by CVD but also by thermal oxidation. As compared to a CVD oxide film, the oxide film formed by thermal oxidation provides the larger effects of preventing peel-off of the silicide film.

[0054]

An oxide film formed by thermally oxidizing a substrate has a better interface state between the substrate and oxide film thana VD oxide film. The silicon nitride film formed between the thermally oxidized film and substrate can improve the MOS transistor characteristics and reliability more than a CVD oxide film formed between the substrate and silicon nitride film.

JP-A-61-16571 describes a lamination structure of an oxide film and a nitride film formed on a gate electrode which has a nitride film side wall. According to this publication, an oxide film is not formed on the side wall of the gate electrode and the nitride film and gate electrode are in direct contact, which is quite different from the present invention. The problem associated with the polycide structure is not described.

[0055]

The second embodiment of JP-A-56-27971 described the structure that the upper and side wall of the gate electrode are covered wit an oxide film and nitride film. However, the oxide film is not formed under the nitride film on the gate electrode side wall. This structure is different from the present invention and the MOS transistor characteristics cannot be expected to be improved. This publication does not describe the problems associated with polycide structure and the nitride film formed on polycide.

[0056]

JP-A-61-194779 describes the structure of the upper surface and side wall of a gate electrode covered with an oxide film and a nitride film. This publication does not describe the problems associated with polycide structure and the nitride film directly formed on polycide.

JP-A-62-261145 describes a composite film made of an oxide film and a silicon nitride film formed around a wiring layer having a polycide structure. However, the object of the invention described in this publication is to use a silicon nitride film in order to prevent metal contamination from a silicide film formed by sputtering. This is quite different from the nitride side wall SAC structure of the present invention.

[0057]

This publication describes that the silicon nitride film is formed under the oxide film and that a

direct contact between the silicon nitride film and polycide poses not problem. This publication does not describe the problem of peel-off of the silicide film on which the nitride film is directly formed. The effects of preventing peel-off by forming the oxide film between the silicide film and nitride film are not described.

In this publication, the composite film of the oxide film and silicon nitride film is formed by patterning a polycide structure. This is different from the present invention. Namely, after an oxide film and a silicon nitride film are formed on polycide, these films are patterned and then a side wall oxide film and silicon nitride film are formed.

[0058]

Another different point of the present invention from the above-cited five publications resides in that the thickness of an oxide film on a polycide electrode is made thicker than an oxide film formed on the electrode side wall so that the effects of preventing peel-off of the nitride film can be increased. The above-cited five publications does not describe this point.

[0059]

The five known examples are quite different from the present invention and do not teach the present invention.

According to the second aspect of the present invention, the above-described problems can be solved by

the semiconductor devices characterized as in the following. A semiconductor device comprising: a plurality of first conductive layers disposed on a substrate generally in parallel; a first insulating film formed on the first conductive layers; a second insulating film made of a silicon nitride film and formed on the first insulating film; a first contact window formed in and through the first and second insulating films between the plurality of first conductive layers; a second conductive layer formed in the first contact window; a third insulating film having etching characteristics different from a silicon nitride film and formed on the second insulating film made of the silicon nitride film; a second contact window formed in the third insulating film at the position over the second conductive layer; and a third conductive layer connected to the second conductive layer via the second contact window.

[0060]

A semiconductor device comprising: a gate electrode of a MIS transistor formed on a gate insulating film on a semiconductor substrate; first and second impurity diffusion regions constituting source and drain of the MIS transistor formed in the semiconductor substrate on both sides of the gate electrode; a first insulating film formed on the semiconductor substrate inclusive of the gate electrode and the first and second impurity diffusion regions; a

second insulating film of a silicon nitride film formed on the first insulating film; a first contact window formed in and through the first and second insulating films and reaching the first impurity diffusion region; a second contact window reaching the second impurity diffusion region; a second conductive layer formed in the first contact window and connected to the first impurity diffusion region; a third conductive layer formed in the second contact window and connected to the second impurity diffusion region; a third insulating film formed on the second insulating film inclusive of the second and third conductive layers; a third contact window formed through the third insulating film and reaching the second conductive layer; and a fourth conductive layer connected to the second conductive layer via the third contact window.

[0061]

The semiconductor device further comprising: a fourth contact window formed through the third insulating film and reaching the third conductive layer connected to the second impurity diffusion region; a fifth conductive layer constituting a storage electrode connected to the third conductive layer via the fourth contact window; and a sixth conductive layer constituting an opposing electrode formed to face the fifth conductive layer, with a capacitor insulating film being interposed between the fifth and sixth conductive layers.

[0062]

The above-described problems can be solved by the semiconductor device manufacture method characterized as in the following.

A manufacture method comprising the steps of: forming a gate insulating film and a first conductive layer on a semiconductor substrate and patterning the first conductive layer to form gate electrodes of MIS transistors; forming impurity diffusion regions constituting source and drain regions in the semiconductor substrate by using the gate electrodes as a mask; forming a first insulating film on the semiconductor substrate inclusive of the gate electrodes; forming a second insulating film made of a silicon nitride film on the first insulating film; selectively and sequentially etching the second and first insulating films to form first contact windows reaching at least ones of the impurity diffusion regions; forming second conductive layers in the first contact windows; forming a third insulating film on the second insulating film inclusive of the second conductive layers; forming second contact windows through the third insulating film, the second contact windows being connected to the second conductive layers; and forming third conductive layers connected to the second conductive layers via the second contact windows.

[0063]

According to the second aspect of the present

invention, the nitride film functioning as an etching stopper layer is formed around the wiring conductive layer formed in the contact window. Therefore, the underlying interlayer insulating films such as the oxide film and BPSG film are not exposed. Even if there is a position misalignment when a contact window is formed in the upper interlayer insulating film formed on the nitride film, the underlying insulating film near the conductive layer is not etched. A process with a large margin for position misalignment is therefore possible.

[0064]

If the contact window is formed at the side of the upper wiring layer, the underlying insulating film is not etched so that a SAC process is possible.

According to the third aspect of the invention, the above-described problems can be solved by providing the semiconductor devices characterized as in the following.

A semiconductor device comprising: a gate electrode of a MIS transistor formed on a gate insulating film on a semiconductor substrate; first and second impurity diffusion regions constituting source and drain of the MIS transistor formed in the semiconductor substrate on both sides of the gate electrode; a first insulating film formed on the semiconductor substrate inclusive of the gate electrode and the first and second impurity diffusion regions; a second insulating film of a silicon nitride film formed

on the first insulating film; a first contact window formed in and through the first and second insulating films and reaching the first impurity diffusion region; a second contact window reaching the second impurity diffusion region; a second conductive layer formed in the first contact window and connected to the first impurity diffusion region; a third conductive layer formed in the second contact window and connected to the second impurity diffusion region; a third insulating film formed on the second insulating film inclusive of the second and third conductive layers; a third contact window formed through the third insulating film and reaching the second conductive layer; and a fourth conductive layer connected to the second conductive layer via the third contact window.

[0065]

A semiconductor device comprising: a gate electrode of a MIS transistor formed on a gate insulating film on a silicon substrate; impurity diffusion regions constituting a source and a drain of the MIS transistor formed in the semiconductor substrate on both sides of the gate electrode; a first insulating film formed on the semiconductor substrate inclusive of the gate electrode and the impurity diffusion regions; a first contact window formed through the first insulating film and reaching at least one of the impurity diffusion regions; a second conductive layer formed in the first contact window and connected to one of the impurity

diffusion regions; a second insulating film formed on the first insulating film inclusive of the second conductive layer; a third insulating film of a silicon nitride film formed on the second insulating film; a second contact window formed in and through the second and third insulating films and connected to the impurity diffusion regions; a third conductive layer constituting a storage electrode connected to the second conductive layer via the second contact window, the third conductive layer having a bottom portion and a cylindrical portion vertical to the semiconductor substrate; and a fourth conductive layer facing the third conductive layer with a capacitor insulating film being interposed therebetween, part of the fourth conductive layer being in contact with the surface of the third insulating film via the capacitor insulating film.

[0066]

The above-described problems can be solved by providing the semiconductor device manufacture methods characterized as in the following.

A manufacture method comprising the steps of: forming a gate insulating film and a first conductive layer on a semiconductor substrate and patterning the first conductive layer to form gate electrodes of MIS transistors; forming impurity diffusion regions constituting source and drain regions in the semiconductor substrate by using the gate

electrodes as a mask; forming a first insulating film on the semiconductor substrate inclusive of the gate electrodes; forming a second insulating film made of a silicon nitride film on the first insulating film; selectively and sequentially etching the second and first insulating films to form first contact windows reaching at least ones of the impurity diffusion regions; forming second conductive layers in the first contact windows; forming a third insulating film on the second insulating film inclusive of the second conductive layers; forming second contact windows through the third insulating film, the second contact windows being connected to the second conductive layers; and forming third conductive layers connected to the second conductive layers via the second contact windows.

[0067]

The method further comprising the steps of: forming a fourth insulating film on the whole surface of the substrate; forming a third contact window reaching the second conductive layer, by selectively removing the fourth and third insulating films on the second conductive layer where the third conductive layer is not formed; selectively forming a fourth conductive layer on the bottom and side wall surfaces of the third contact window; removing the fourth insulating film by using the fourth conductive layer as a mask and the second insulating film as an etching stopper to expose the fourth conductive layer in a cylindrical shape; forming

a fifth insulating film on the surface of the fourth conductive layer; forming a fifth conductive layer on the semiconductor substrate inclusive of the fifth insulating film; and selectively removing the fifth conductive layer by leaving at least part of the fifth conductive layer inclusive of the fourth conductive layer.

[0068]

The method further comprising the steps of: forming a sixth insulating film of a silicon nitride film covering the upper surface and side wall of the third conductive layer; and removing the fourth insulating film by using the second and sixth insulating films as an etching stopper.

A method of manufacturing a semiconductor device comprising the steps of: sequentially forming on a semiconductor substrate a first conductive layer, a first insulating film, a second insulating film made of silicon nitride, and a third insulating film; forming a contact window reaching the first conductive layer by sequentially etching the third, second, and first insulating films; selectively forming a second conductive film on the bottom and side wall of the contact window; removing the third insulating film by using the second conductive layer as a mask and the second insulating film as an etching stopper to expose the second conductive layer of cylindrical shape; forming a fourth insulating film on the surface of the

second conductive film; forming a third conductive layer on the semiconductor substrate inclusive of the fourth insulating film; and selectively removing the third conductive layer leaving at least part of an area inclusive of the second conductive layer.

[0069]

A manufacture method comprising the steps of: forming a gate insulating film and a first conductive layer on a semiconductor substrate, and patterning the first conductive layer to form a gate electrode of a MIS transistor; forming impurity diffusion regions constituting a source and a drain in the semiconductor substrate by using the gate electrode as a mask; forming a first insulating film on the semiconductor substrate inclusive of the gate electrode; selectively etching the first insulating film to form first contact windows reaching the impurity diffusion regions; forming second conductive layers in the first contact windows; forming a second insulating film on the first insulating film inclusive of the second conductive layers; forming a second contact window through the second insulating film to expose one of the second conductive layers; forming a third conductive layer connected to one of the second conductive layers via the second contact window; sequentially forming on the semiconductor substrate inclusive of the third conductive layer a third insulating film, a fourth insulating film made of silicon nitride, and a fifth insulating film;

selectively removing the fifth, fourth, third, and second insulating films over the other of the second conductive layer where the third conductive layer is not formed, to form a third contact window reaching the other of the second conductive layer; selectively forming a fourth conductive layer on the bottom and side wall of the third contact window; removing the fifth insulating film by using the fourth conductive layer as a mask and the fourth insulating film as an etching stopper to expose the fourth conductive layer of cylindrical shape; forming a sixth insulating film on the surface of the fourth conductive layer; forming a fifth conductive layer on the semiconductor substrate inclusive of the sixth insulating film; and selectively removing the fifth conductive layer leaving at least part of an area inclusive of the fourth conductive layer.

[0070]

According to the third aspect of the present invention, when a cylinder type storage electrode is formed, the nitride film functioning as an etching stopper film is formed under the insulating film at the outer side of the storage electrode. Therefore, the insulating film at the outer side of the storage electrode can be completely removed. It is possible to make constant the outer surface area of the cylinder type storage electrode. Variation in capacitance becomes small so that stable DRAM cells can be manufactured.

[0071]

DRAM cells can be manufactured not to make too large a height difference between the cell area and peripheral circuit area.

According to the fourth aspect of the invention, the above-described problems can be solved by providing the semiconductor devices characterized as in the following.

A semiconductor device comprising: first and second conductive layers formed at levels different in distance from the substrate surface, the levels becoming higher in the order of the first and second conductive layers; a first insulating film formed on the substrate, covering the first and second conductive layers; a first contact window formed through the first insulating film and exposing the top surface of the first conductive layer; a second contact window formed in and through the first insulating film and the second conductive layer, the second conductive layer having a side wall exposed in the second contact window; and a pair of third conductive layers formed at least in the first and second contact windows and connected via the first contact window to the surface of the first conduction layer and to the side wall of the second conductive layer via the second contact window, wherein D1 is larger than D2, where D1 is a depth from the surface of the first insulating film to the first conductive layer and D2 is a depth from the surface of the first

insulating film to the second conductive layer.

[0072]

A semiconductor device comprising: first to third conductive layers formed at levels different in distance from a substrate surface; a first insulating film formed on the substrate inclusive of the first to third conductive layers; a second insulating film formed under the second conductive layer and having etching characteristic different from the first insulating film; a third insulating film formed on the third conductive layer and having etching characteristics same as the second insulating film; a first contact window formed through the first insulating film and exposing the top surface of the first conductive layer; a second contact window formed through the first insulating film, the second conductive layer, and the second insulating film; a third contact window formed through the first and third insulating films and exposing the surface of the third conductive layer; and fourth conductive layers respectively connected to the surface of the first conductive layer via the first contact window, to the side wall of the second conductive layer via the second contact window, and to the surface of the third conductive layer via the third contact window, wherein D1 > D3 > D2, where D1 is a depth from the surface of the first insulating film to the first conductive layer, D2 is a depth from the surface of the first insulating film to the second conductive layer, and D3 is a depth

from the surface of the first insulating film to the third conductive layer.

[0073]

The above-described problems can be solved by providing the semiconductor device manufacture methods characterized as in the following.

A method of manufacturing a semiconductor device comprising the steps of: forming first conductive layers on a semiconductor substrate; forming a first insulating film on the first conductive layers; forming second conductive layers on the first insulating film; forming a second insulating film on the semiconductor substrate inclusive of the second conductive layers; forming a mask on the second insulating film for forming contact windows; and sequentially etching the second and first insulating films by using the mask to form a contact window over the first conductive layer and sequentially etching the second insulating film and second conductive layer by using the mask to form a contact window through the second conductive layer.

[0074]

A method of manufacturing a semiconductor device comprising the steps of: forming first conductive layers on a semiconductor substrate; sequentially forming a first insulating film and a second insulating film made of a silicon nitride film on the first conductive layers; forming a second conductive layer on the second insulating film; selectively removing the second

insulating film at least at an area of a contact portion of one of the first conductive layers; forming a third insulating film on the semiconductor substrate inclusive of the second insulating film, the first insulating film, and the semiconductor substrate; forming a mask on the third insulating film for forming contact windows; and sequentially etching the third and first insulating films by using the mask to form a contact window over the first conductive layer and sequentially etching the third insulating film and second conductive layer by using the mask to form a contact window penetrating through the second conductive layer.

[0075]

According to the fourth aspect of the invention, when a contact window is formed through a plurality of wiring layers, the nitride film is formed under the upper wiring layer to etch the wiring layers by using the nitride film as a stopper. It is therefore possible to prevent the contact window from being etched from the upper wiring layer to the insulating layer under the nitride film and reaching the lower wiring layer. It is therefore possible to prevent an electric short between layers. It is possible to form contact windows having different depths in the upper and lower wiring layers by a single photolithography process. The number of processes can be reduced.

[0076]

A first etching step is performed by using as a

stopper a nitride film formed on the intermediate wiring layer between the upper and lower wiring layers. Next, a second etching step is performed to etch the nitride film. It is possible to prevent the contact window from being etched from the upper wiring layer to the insulating layer under the nitride film or from the intermediate wiring layer to the lower insulating layer, and reaching the lower wiring layer. It is therefore possible to prevent an electric short between layers. It is possible to form contact windows having different depths in the upper, intermediate and lower wiring layers by a single photolithography process. The number of processes can be reduced.

[0077]

According to the fifth aspect of the invention, the above-described problems can be solved by providing the semiconductor devices characterized as in the following.

A semiconductor device comprising: a plurality of first conductive layers formed on the surface of a semiconductor substrate generally in parallel; first insulating films formed to cover the first conductive layers; a second insulating film embedded between adjacent ones of the first conductive layers, the second insulating film having a surface coincident with the upper surface of the first insulating films and parallel to the surface of the semiconductor substrate; and a contact window formed in the second insulating film,

part of the contact window riding upon one of the first insulating films.

[0078]

A semiconductor device comprising: a plurality of first conductive layers formed on the surface of a semiconductor substrate generally in parallel and having a plurality of levels different in distance from the surface of the semiconductor substrate; first insulating films formed to cover the first conductive layers; and a second insulating film embedded between adjacent ones of the first conductive layers and having a surface coincident with the upper surface of the first insulating films with the highest level in distance from the surface of the first insulating film and parallel to the surface of the semiconductor substrate.

[0079]

The semiconductor device further comprising a contact window formed in the second insulating film, part of the contact window extending to an area over one of the first insulating films.

In the semiconductor device, the first insulating films are each made of a silicon nitride film.

[0080]

The above-described problems can be solved by providing the semiconductor device manufacture method characterized as in the following.

A method of manufacturing a semiconductor device comprising the steps of: sequentially forming a first

conductive layer and a first insulating film on a semiconductor substrate; patterning a lamination of the first insulating film and the first conductive layer into lamination units disposed generally parallel; forming a second insulating film on the semiconductor substrate inclusive of the lamination units and anisotropically etching the lamination units to form side spacers on side walls of the lamination units; forming a third insulating film on the semiconductor substrate inclusive of the first conductive layer covered with the first and second insulating films; planarizing the third insulating film by CMP by using the first insulating film as a stopper; and partially removing the third insulating film to form a contact window, part of the bottom of the contact window extending at least over part of the second insulating film.

[0081]

A method of manufacturing a semiconductor device comprising the steps of: forming an element isolating insulating film on a semiconductor substrate to define an active region; sequentially forming a first conductive layer and a first insulating layer on the semiconductor substrate inclusive of the element isolating insulating film and the active region; patterning a lamination of the first insulating film and the first conductive layer into lamination units disposed generally parallel; forming a second insulating

film on the semiconductor substrate inclusive of the lamination units and anisotropically etching the lamination units to form side spacers on side walls of the lamination units; forming a third insulating film on the semiconductor substrate inclusive of the first conductive layer covered with the first and second insulating films and the element isolating insulating film; and planarizing the third insulating film by CMP by using the first insulating film on the element separation insulating film as a stopper.

[0082]

According to the fifth aspect of the present invention, when the insulating film on the wiring layer group used by nitride film spacer SAC is planarized, the nitride film is used as a CMP stopper. Planarizing can be performed by newly forming a stopper film. Without increasing the number of processes, planarizing with high precision is therefore possible.

In the process of planarizing the insulating film formed on the wiring layer group having different distances from the substrate, the nitride film on the wiring layer group having the longest distance from the substrate is used as a CMP stopper. The insulating film on the wiring layer group can be planarized with high precision.

[0083]

The film under the insulating film on the wiring group not having the longest distance from the substrate

is not subjected to polishing as the stopper. A predetermined thickness and breakdown voltage can be maintained.

JP-A-6-181209 discloses that a silicon nitride film is formed on the upper surface of a conductive layer and an insulating film is formed on the silicon nitride film which is used as a CMP stopper. Fig. 4 of this publication shows as conventional techniques that a silicon nitride film is formed on the upper and side wall of conductive layers patterned in a predetermined shape and in between the conductive layers and that the silicon nitride film is used as a CMP stopper film.

[0084]

However, this publication does not describe nitride spacer SAC and the problem associated with nitride film spacer SAC used by DRAM.

In the DRAM manufacture method of the invention, the nitride film on the conductive layer is used as a stopper layer. It is therefore possible to planarize the insulating film formed on the upper layer and to suppress a variation in film thicknesses.

[0085]

If there is a variation in thicknesses of planarized films, there is a distribution of etching amounts when contact holes are formed at a later process by nitride film spacer SAC, and the nitride film area is reduced when the contact hole is formed. There arises a large possibility that the conductive layer and an upper

conductive layer formed in the contact window are electrically shorted.

According to the present invention, the nitride film space necessary for nitride film spacer SAC is used without newly forming a stopper layer. A new process is not necessary.

[0086]

The above-described know example does not describe the problem specific to the nitride film spacer SAC used for DRAM and does not teach any means for solving this problem.

According to the present invention, of wiring layers having different distances from the substrate, the nitride film on only the wiring layer having the longest distance from the substrate is used as a stopper, and the nitride film on the wiring layer having a shorter distance from the substrate is not used as a stopper. Therefore, the breakdown voltage of the nitride film on the wiring layer near the substrate can be prevented from being lowered. The publication does not describe such point in any paragraph.

[0087]

According to the sixth aspect of the invention, the above-described problems can be solved by providing the semiconductor devices characterized as in the following.

A semiconductor device comprising: a gate electrode of a MIS transistor formed on a gate

insulating film on a silicon substrate; first and second impurity diffusion regions constituting source and drain of the MIS transistor formed in the silicon substrate on both sides of the gate electrode; an insulating film formed on the silicon substrate inclusive of the gate electrode and the first and second impurity diffusion regions; a pair of contact windows formed in and through the insulating film and reaching the first and second impurity diffusion regions; first and second conductive layers made of the same conductive layer and connected to the first and second impurity diffusion regions via the contact windows; a bit line connected to the first impurity diffusion area via the first conductive layer; and a capacitor storage electrode connected to the second impurity diffusion region via the second conductive layer, wherein the impurity concentration of the second impurity diffusion region is larger than the impurity concentration of the first impurity diffusion region.

[0088]

A semiconductor device comprising: a gate electrode of a MIS transistor formed on a the gate insulating film on a silicon substrate; first and second impurity diffusion regions constituting source and drain of the MIS transistor, having the same impurity concentration and formed in the silicon substrate on both sides of the gate electrode; an insulating film formed on the silicon substrate inclusive of the gate

electrode and the first and second impurity diffusion regions; a pair of contact windows formed through the insulating film and reaching the first and second impurity diffusion regions; a third impurity diffusion region of the same conductivity type as the second impurity diffusion region formed in the silicon substrate under the contact window merging with the second impurity diffusion region, the impurity concentration of the third impurity diffusion region being larger than the impurity concentrations of the first and second impurity diffusion regions; a first conductive layer connected to the first impurity diffusion area via one of the contact windows; a second conductivity layer made of the same conductive layer as the first conductive layer and connected to the second impurity diffusion region and the third impurity diffusion region via the other of the contact windows; a bit line connected to the first impurity diffusion region via the first conductive layer; and a capacitor storage electrode connected to the second impurity diffusion region via the second conductive layer, wherein the impurity concentration of the third impurity diffusion region is larger than the impurity concentration of the first and second impurity diffusion regions.

[0089]

The above-described problems can be solved by providing the semiconductor device manufacture method

characterized as in the following.

A method of manufacturing a semiconductor device comprising the steps of: forming a gate oxide film and a gate electrode on a semiconductor substrate of a first conductivity type; implanting first impurity ions of a second conductivity type opposite to the first conductivity type into the semiconductor substrate by using the gate electrode as a mask to form first and second impurity diffusion regions constituting source/drain regions; forming an insulating film on the semiconductor substrate covering the gate electrode; partially etching the insulating film to form a first contact window reaching the first impurity diffusion region and a second contact window reaching the second impurity diffusion region; covering the second contact window with a mask pattern; implanting second impurity ions of the second conductivity type into the first impurity diffusion region exposed in the first contact window by using the mask pattern and the insulating film as a mask to form a third impurity diffusion region; forming a first conductive layer connected to the third and first impurity diffusion regions via the first contact window and a second conductive layer connected to the second impurity diffusion region via the second contact window; forming a DRAM storage electrode connected to the third and first impurity diffusion regions via the first conductive layer; and forming a DRAM bit line connected to the second impurity diffusion

regions via the second conductive layer.

[0090]

In the method, a dose of second conductivity ion implantation is larger than a dose of first conductivity ion implantation.

According to the sixth aspect of the invention, impurities for preventing junction leak are implanted only into the source/drain region on the capacitor side of the memory cell area, and impurities for preventing junction leak are not implanted into the source/drain region on the bit line connection side.

[0091]

Since impurities are implanted only into the source/drain region on the capacitor connection side, one of the source/drain regions of a MOS transistor can have a shallow junction. It is possible to suppress the short channel effects of transistors and adverse effects of leak current upon elements. The junction leak which is severe on the capacitor connection side can be suppressed.

[0092]

Embodiments of the Invention]

Embodiments will be described hereinbelow. Identical reference numerals are used in each embodiment for same or similar elements.

[1st Embodiment]

Fig. 2 is a schematic plan view of a DRAM memory cell area. In Fig. 2, reference numeral 11 represents

an active region, reference numeral 12 represents a word line of MOS transistors also serving as gate electrodes, reference numeral 13 represents a bit line, reference numeral 14 represents a contact window for contact between the bit line and source/drain diffusion region of a MOS transistor, and reference numeral 15 represents a contact window for contact between a cylinder type storage electrode and source/drain region of a MOS transistor. Wiring layers such as back-up wiring lines formed on gate electrodes or bit lines are not shown in Fig. 2.

[0093]

Next, with reference to Figs. 3 to 13, a method of forming contact windows of DRAM by self align contact (SAC) techniques will be specifically described. Figs. 3 to 13 are schematic cross sectional views showing a memory cell area taken along line A-A' of Fig.2 and a typical wiring structure of a peripheral circuit area.

First, as shown in Fig. 3(a), on a p-type silicon substrate 16, a thick oxide film (field oxide film) 17 is formed by well known LOCOS (local oxidation of silicon) to thereby define element isolation regions and active regions. Reference characters MC represent a memory cell area, and PC represents a peripheral circuit area.

[0094]

Various circuits are formed in the peripheral circuit area. For these circuits, n- and p-channel MOS

transistor regions are generally formed in this area.

The p-channel MOS transistor area may be an n-type well formed in a p-type silicon substrate, and the n-channel MOS transistor area may be a p-type well formed in the p-type silicon substrate or a p-type well (triple-well structure) formed in an n-type well in the p-type silicon substrate. These structures may be selected as desired according to the design characteristics.

[0095]

Although not shown, after or before LOCOS, p-and n-type impurity ions are implanted into the active regions of the peripheral circuit area to form p- and n-type wells. In a partial area of each n-type well, p-type impurities are doped to form a p-type well whose bottom and side are surrounded by the n-type well.

[0096]

If necessary, channel stopper regions are formed under the field oxide film 17 by implanting p- or n-type impurity ions depending upon the conductivity type of impurities in wells.

Although not shown, impurities for the control of threshold values (Vth) are doped in the active regions depending on the characteristics of MOS transistors.

[0097]

Ion implantation processes for these wells, channel stopper regions, and Vth control are not required to be executed at this stage, but obviously

they may be executed after a gate oxide film forming process, a gate electrode forming process, or the like which will be later described sequentially.

Next, as shown in Fig. 3(b), the substrate surface is oxidized to form a gate oxide film 18 which is 8 nm thick. On this gate oxide film 18, a phosphorous doped silicon film 19 having a thickness of 50 nm, a tungsten silicide (WSi) film 20 having a thickness of 50 nm, and a silicon nitride film 21 having a thickness of 80 nm are sequentially deposited by well known CVD (chemical vapor deposition).

[0098]

The lamination of these films is patterned to a desired shape by photolithography to form MOS transistor gate structures. In the cell area, the polycide structure of the lamination becomes the word line (corresponding to 12 in Fig. 1).

Next, as shown in Fig. 4(a), heat treatment in an oxidizing atmosphere is performed to thermally grow an oxide film 22 to 2 to 10 nm thick. This oxidation forms an oxide film only on the side wall of the polycide structure of the silicon film 19 and WSi film 20 and on the surface of the silicon substrate 16 at the active region. This oxide film is not formed on the surface of the silicon nitride film 21 including its side wall because the silicon nitride film 21 is not oxidized. Since the silicon film 19 has an impurity concentration higher than the substrate 11, the oxide film 22 on the

side wall of the silicon film 19 becomes thicker than on the substrate surface.

[0099]

Next, by using the gate electrode structure as a mask, n-type impurity ions, phosphorous, are doped at a dose of 1 x $10^{13}cm^{-2}$ over the whole surface of the substrate. An impurity doped region 23 corresponding to an n--type region of an LDD (lightly doped drain) structure is therefore formed in the n-channel MOS transistor region.

In this case, these n-type impurities are also doped in the p-channel MOS transistor region. However, this region substantially disappears at the later process of high concentration p-type impurity ion implantation so that there is no practical problem. Further, if this n-type impurity region is controlled to be left at the periphery of the p-type impurity diffusion region serving as a source/drain region, it functions as a punch-through preventing region.

[0100]

Next, as shown in Fig. 4(b), a silicon nitride film is deposited by CVD to a thickness of 50 to 150 nm and anisotropically etched by well known RIE (reactive ion etching) to form a nitride film side wall spacer on the side wall of the gate electrode.

In this case, it is preferable that the etching is stopped by leaving the oxide film 22 not covered with the nitride film 21 present on the substrate 16 or the

like, because etching damages to the substrate can be suppressed. However, it is not always required to leave it.

[0101]

This side wall nitride film becomes in unison with the nitride film 20 on the polycide electrode and continuously covers the upper surface and side surface of the gate electrode, forming a nitride film region 24.

At this process, although the periphery of the polycide electrode made of the silicon film 19 and WSi film 20 is covered with the nitride film region 24, the oxide film 22 exists on the side wall of the polycide electrode. It is therefore possible to prevent the WSi film 20 from being separated from the substrate at later heat treatments or and the like.

[0102]

Next, an oxide film is grown to 2 to 10 nm by thermal oxidation. In this case, this oxidation may be performed after removing the oxide film 22 exposed over the silicon substrate by hydrofluoric acid containing etchant. Although it is preferable to remove this exposed oxide film, from the viewpoint of controllability of film thickness, there is a danger of etching also the field oxide film 17 and the oxide film 22 under the side wall nitride film.

With this oxidation, mainly the surface of the active region of the silicon substrate is oxidized and this oxidized film becomes in unison with the oxide film

22. The silicon film 19 and WSi film 20 covered with the nitride film region 24 are not oxidized. In this embodiment, this unified oxide film is collectively called hereinafter an oxide film 22.

[0103]

Next, a resist pattern is formed exposing the n-channel MOS transistor region in the peripheral circuit area excepting the memory cell area. By using the gate electrodes with the nitride film region 24 as a mask, n-type impurity ions, arsenic, are implanted at a dose of $5 \times 10^{15}cm^{-2}$ into the opening area of the resist pattern. In the n-channel MOS transistor region in the peripheral circuit area, an impurity diffusion region 25 of high concentration is formed as the n+-layer of the LDD structure.

[0104]

The reason why n-type impurity ions are not implanted into the source/drain regions of transistors in the memory cell area is to prevent crystal detects to be formed by implantation of ions at a high impurity concentration and suppress leak current from a capacitor which stores small electric charges.

Next, a resist pattern is formed exposing the p-channel MOS transistor region in the peripheral circuit area. By using the gate electrodes with the nitride film region 24 as a mask, BF_2^+ ions are implanted at a dose of $5 \times 10^{15}cm^{-2}$ into the opening area of the resist pattern to form an impurity diffusion region serving as

a source/drain region of the p-channel MOS transistor.

[0105]

Next, as shown in Fig. 5A, a BPSG film 26 is grown to a thickness of 100 to 200 nm by CVD, and thereafter, heat treatment is performed at a temperature of 750 to 900 °C to planarize the surface of the BPSG film 26 through reflow.

Etch-back or CMP may be used to further planarize the surface, or a combination of these processes may be used for planarization.

[0106]

If etch-back or CMP is used, the BPSG film is grown thicker correspondingly by an amount to be removed, in order to set the film thickness after etch-back or CMP to 100 to 200 nm.

Next, a resist pattern is formed having an opening which exposes the source/drain regions of a MOS transistor in the memory cell area. By using this resist pattern as a mask, the BPSG Film 26 and oxide film 22 exposed in the opening are sequentially etched by RIE using, for example, mixed gas of C_4F_8 and CO to thereby expose the substrate surface and form a contact window 27.

[0107]

The bottom of the contact window 27 is defined in a self alignment manner by the spacer of the nitride film region 24. Since the side surface of the polycide gate electrode is all covered with the nitride film and

the oxide film is not exposed, the oxide film is not etched and removed even if there is misalignment of the opening of the resist pattern. Therefore, the gate electrode and contact electrode will not be electrically shorted as in the case of conventional techniques described with Fig. 35.

[0108]

Etching the BPSG film 26 and oxide film 22 is preferably performed under the conditions that an etching selection ratio of the BPSG film 26 and oxide film 22 to the nitride film is 10 or higher so as not to etch the nitride film region 24.

Next, after the resist pattern is removed, by using the BPSG film 26 and nitride film region 24 as a mask, n-type impurity ions, phosphorus, are implanted at a dose of $3 \times 10^{13}cm^{-2}$ into the silicon substrate exposed in the contact window 27 to thereby form an n-type diffusion region 28.

[0109]

Although this n-type diffusion region 28 is not necessarily required, presence of this region solves a problem of large junction leak near at the edge portion of the field oxide film 17 where n-type impurities for forming the source/drain region are not implanted, even if the contact hole 27 is displaced and formed riding over the edge portion of the field oxide film 17.

[0110]

Next, as shown in Fig. 5(b), a phosphorus doped

silicon film is formed by CVD over the whole surface of the substrate, and a plug 29 of the silicon film is left in the contact hole 27 by etch-back or CMP.

The plug 29 of silicon may be formed by selective CVD without using etch-back or CMP.

[0111]

An oxide film 30 is then formed by CVD to a thickness of 30 to 100 nm.

Next, as shown in Fig. 6(a), a resist pattern having an opening at a bit line connection area is formed. By using this resist pattern as a mask, the oxide film 30 is etched to form a contact window 31 exposing part of the upper surface of the silicon plug 29. Thereafter, the resist pattern is removed.

Next, a phosphorus doped silicon film 32 of 30 nm thick, a WSi film 33 of 50 nm thick, and a silicon nitride film 24 of 80 nm thick are sequentially formed by CVD.

[0112]

The lamination of these films is patterned to have a desired wiring pattern by well know photolithography. The polycide electrode of this lamination forms a bit line (13 in Fig. 2) in the memory cell area, and is also used as a wiring layer other than the bit line in the peripheral circuit area.

Next, as shown in Fig. 6(b), an oxide film 35 is grown to a thickness of 2 to 10 nm by thermal oxidation. The oxide film is therefore formed on the side wall of

the polycide structure of the silicon film 32 and WSi film 33. Since the silicon nitride film is not oxidized, no oxide film is formed on the side wall of the silicon nitride film 34.

[0113]

A silicon nitride film is formed to a thickness of 50 to 150 nm and anisotropically etched by RIE to form a spacer of nitride on the side wall of the bit line.

The sidewall nitride film is made in unison with the nitride film 34 on the polycide electrode and becomes a nitride film region 36 continuously covering the upper surface and side surface of the polycide electrode.

[0114]

With the above process, the periphery of the polycide electrode of the silicon film 32 and WSi film 33 is covered with the nitride film region 36. Since the oxide film 35 is formed on the side wall of the polycide electrode, the WSi film 33 can be prevented from being separated from the substrate, at later heat treatments or the like.

Next, as shown in Fig. 7, a BPSG film 37 is grown to a thickness of 500 nm by CVD, and thereafter heat treatment is performed at a temperature of 750 to 900 °C to planarize the surface thereof by reflow.

[0115]

For further planarization, etch-back or CMP may be used or a combination thereof may be used.

If etch-back or CMP is used, the BPSG film is grown thicker correspondingly by an amount to be removed, to thereby set the film thickness after etch-back or CMP to 500 nm.

[0116]

The thickness of the BPSG film 37 is one of the factors which determine the capacitance of a memory capacitor if the cylinder type storage electrode is used. Therefore, if a large capacitance is necessary, the film thickness of the BPSG film 37 is made thicker than 500 nm.

Next, as shown in Fig. 8, a resist pattern having an opening exposing a capacitor connection area is formed. By using this resist pattern as a mask, the BPSG film 37 and oxide film 30 are sequentially etched by RIE using, for example, mixed gas of C_4F_8 and CO to form a contact window 38 exposing the upper surface of the silicon plug 29.

[0117]

If a cylinder type storage electrode is used, the size of the contact window 38 is generally related to the bottom area and its circumferential length of the cylinder type storage electrode. Therefore, in order to increase the capacitance, it is desired to form a contact window as large as possible.

In this embodiment, the contact window 38 is defined in self alignment with the bit line because of the nitride film region 36. Therefore, the contact

window can be extended to the upper portion of the polycide electrode serving as the bit line so that the bottom area and its circumferential length can be increased.

[0118]

Furthermore, since the periphery of the polycide electrode is completely covered with the nitride film region 36 which is not etched and removed, the bit line and storage electrode are not electrically shorted.

Etching the BPSG film 37 and oxide film 30 is preferably performed under the conditions that the etching selection ratio of the BPSG film 37 and oxide film 30 to the nitride film is 10 or higher.

[0119]

Next, as shown in Fig. 9, after the resist pattern is removed, a phosphorous doped silicon film is formed by CVD to a thickness of 50 nm and etched by etch-back or CMP to leave a silicon film 39 only on the side wall and bottom of the contact window 38.

Next, as shown in Fig. 10, the BPSG film 37 is etched by hydrofluoric acid containing etchant and left for a thickness of, for example, 150 nm. In this state, a hollow cylinder type storage electrode 39 is formed.

[0120]

Next, as shown in Fig. 11, a silicon nitride film is formed by CVD to a thickness of 40 nm, and thermally oxidized by 1 to 2 nm to form a capacitor insulating film 39a on the surface of the storage electrode 39 (the

capacitor insulating film is not shown).

Then, as shown in Fig.11, a phosphorous doped silicon film is formed by CVD to a thickness of 50 nm and patterned to form an opposing electrode 40 of the capacitor. At the patterning step, an unnecessary capacitor insulating film is removed at the area outside of the pattern of the opposing electrode 40.

[0121]

Next, as shown in Fig. 12, a BPSG film 41 is grown by CVD to a thickness of 1 μm and subjected to heat treatment at a temperature of 750 to 900 °C to planarize the surface thereof by reflow.

For further planarization, etch-back or CMP may be used or a combination thereof may be used.

[0122]

With the above planarizing process, a difference of height between the memory cell area and peripheral circuit area is very small and generally the flat surface can be obtained.

Next, as shown in Fig. 13, contact windows 42 to 45 are formed. The contact window 42 is used for contact with the opposing electrode 40, the contact hole 43 is used for contact with a wiring layer of the silicon film 32 and WSi film 33 in the peripheral circuit area, the contact hole 44 is used for contact with a wiring layer of the silicon film 19 and WSi film 20 in the peripheral circuit area, and the contact hole 45 is used for contact with the diffusion region 25 of a

MOS transistor in the peripheral circuit area.

[0123]

Since the BPSG film 41 is subjected to the planarizing process, its surface irregularity can be suppressed within the depth of focus of an exposure apparatus used at a resist exposure process. Size accuracy can therefore be prevented from being lowered.

It is desired to open these contact windows 42 to 45 by a single photolithography process in order to reduce the number of processes. However, since the depths of the contact windows are very different, while the contact window 45 for the lowermost diffusion region 25 is formed, the contact window 42 for the uppermost opposing electrode 40 may penetrate through the opposing electrode and at the worst the lower wiring layer is electrically shorted.

[0124]

This problem that the contact window penetrates through the conductive layer can be solved by dividing the window forming process into a plurality of processes for deep and shallow windows. For example, the process of forming the contact windows 42 to 45 is divided into two processes for the opposing electrode and for the other conductive layers, or for the opposing electrode and bit line and for the word line and diffusion region.

[0125]

Next, as shown in Fig. 14, a titanium (Ti) film, a titanium nitride (TiN) film, and a tungsten (W) film are

sequentially formed respectively by sputtering, reactive sputtering, and CVD, and patterned to form a first metal wiring layer 46.

The first metal wiring layer 46 is also disposed in the memory cell area in parallel to the word line, and mainly used for interconnections to a word decoder and a subsidiary word decoder.

[0126]

Although not shown, thereafter, an interlayer insulating film is grown over the first metal wiring layer 46 and planarized by CMP.

After contact windows are formed in the interlayer insulating film over the first metal wiring layer 46, a second wiring layer is formed and patterned. The second metal wiring layer may be a lamination of a TiN film, an aluminum (Al) film, and a TiN film.

[0127]

The second metal wiring layer in the memory cell area is disposed in parallel to the bit line, and mainly used for interconnections to a column decoder and a sense amplifier.

The second metal wiring layer is also used as bonding pads.

Lastly, as a passivation film, a silicon oxide film and a silicon nitride film are sequentially formed by CVD. The passivation film on the bonding pad is etched to complete a DRAM.

[0128]

In this embodiment, the polycide electrode constituting the word line, gate electrode, bit line, and wiring in the peripheral circuit area is covered with the nitride film spacer, and the oxide film is formed on the side wall of the polycide electrode under the nitride spacer. Therefore, the polycide electrode can be prevented from being separated from the substrate at later heat treatments.

Furthermore, the polycide gate electrode is completely covered with the nitride film and the oxide film is not exposed. Therefore, the oxide film is not etched when the self align contact window is formed even with misalignment and therefore the polycide electrode and upper level wiring layer are not electrically shorted.

[0129]

The thicker the oxide film 22 formed on the side wall of the gate electrode, the more resistant against separation of the silicide film. However, if the oxide film 22 is formed by thermal oxidation, the substrate is oxidized at the same time and an oxide film region called a gate bird's beak thicker than the gate oxide film is formed at the opposite ends under the gate electrode. This gate bird's beak may deteriorate the characteristics of MOS transistors. Therefore, the thickness of the oxide film 22 is determined while taken this into consideration.

[2nd Embodiment]

In the first embodiment, the oxide film is formed only on the side wall of the polycide electrode, as shown in Fig. 1(a). In the second embodiment, the structure that the oxide film completely covers the polycide electrode as shown in Fig. 1(b) will be described with reference to Figs. 15 and 16. Similar to the first embodiment, Figs. 15 and 16 are schematic cross sectional views showing a memory cell area taken along line A-A' of Fig. 1 and a typical wiring structure of a peripheral circuit area.

[0130]

Fig. 15 shows an example of a gate electrode and a word line (12 in Fig. 1) to which the structure shown in Fig. 1(b) is applied.

A field oxide film 17 is formed on a p-type silicon substrate 16 by the same method as described with Fig. 3(a).

Next, as shown in Fig. 15(a), the substrate surface is oxidized to form a gate oxide film 18 to a thickness of 8 nm. On this gate oxide film 18, a phosphorous doped silicon film 19 having a thickness of 50 nm and a WSi film 20 having a thickness of 50 nm are sequentially deposited by CVD.

[0131]

Then, an oxide film 47 is formed to a thickness of 3 to 50 nm. This film may be formed either by thermal oxidation or CVD. The thermal oxidation is more preferable because a structure more resistant to

separation or peel-off can be obtained. If the oxide film is formed by thermal oxidation, the polycide film is thinned. In this case, therefore, it is also effective to use a method of forming a thin oxide film by thermal oxidation and thereafter forming an oxide film by CVD to obtain a desired oxide thickness.

[0132]

After a silicon nitride film 21 is formed by CVD to a thickness of 80 nm, the lamination of these films is patterned into a gate electrode and a wiring layer.

As different from the first embodiment, the lamination is formed by the silicon film 19, WSi film 20, oxide film 47, and silicon nitride film 21.

Next, as shown in Fig. 15(b), a heat treatment is performed to grow a thermal oxide film to 2 to 10 nm thick. This oxidation forms an oxide film on the side wall of the polycide structure of the silicon film 19 and WSi film 20, the oxide film becoming in unison with the oxide film 47 to form an oxide film region 48.

[0133]

Then, similar to the first embodiment, by using the gate electrode as a mask, n-type impurity ions, phosphorous, are doped at a dose of $1 \times 10^{13}cm^{-2}$ over the whole surface of the substrate. An impurity doped region 23 corresponding to an n^-type region of an LDD structure is therefore formed in the n-channel MOS transistor region.

Then, a silicon nitride film is formed by CVD to a

thickness of 50 to 150 nm and anisotropically etched to form a nitride film region 24 covering the oxide film region 48.

[0134]

Thereafter, by using the similar processes to the first embodiment, the second DRAM is completed.

In this embodiment, the oxide film is formed not only on the side walls of the silicon film 19 and WSi film 20 but also on the upper surface of the WSi film 20 so that the polycide electrode does not directly contact the silicon nitride film. Therefore, a structure more resistant to separation or peel-off of the WSi film can be obtained.

[0135]

Fig. 16 shows a bit line (13 in Fig. 1) in the memory cell area to which the structure shown in Fig. 1(b) is applied.

The processes similar to the first embodiment are performed up to that shown in Fig. 5(b) to form a silicon oxide film 30 on a planarized BPSG film 26.

As shown in Fig. 16(a), a resist pattern having an opening at the bit line connection area is formed. By using the resist pattern as a mask, the oxide film 30 is etched to form a contact window 31 which exposes part of the upper surface of the silicon plug 29. Thereafter, the resist pattern is removed.

[0136]

Successively, a phosphorous doped silicon film 32

is formed to a thickness of 30 nm, a WSi film 33 is formed by CVD to a thickness of 50 nm, and thereafter an oxide film 49 of 3 to 50 nm is formed. The structure of these films and manufacture methods thereof are the same as those previously described with word lines of the 2nd DRAM.

Next, after a silicon nitride film 21 is formed by CVD to a thickness of 80 nm, the lamination of these films is patterned to form bit lines and a wiring layer.

[0137]

As shown in Fig. 16(b), an oxide film is grown to a thickness of 2 to 10 nm by thermal oxidation. The oxide film is therefore formed on the side wall of the polycide structure of the silicon film 32 and WSi film 33. An oxide film region 50 in unison with the oxide film 49 is therefore formed.

Next, a silicon nitride film is formed by CVD to a thickness of 50 to 150 nm and anisotropically etched by RIE to form a nitride film region 36 covering the oxide film region 48.

[0138]

Thereafter, the processes similar to the first embodiment are performed to complete a DRAM.

Also in this embodiment, similar to the word line, the oxide film is formed not only on the side walls of the silicon film 32 and WSi film 33 but also on the upper surface of the WSi film 33, so that the polycide electrode does not directly contact the silicon nitride

film. A structure more resistant to separation of the WSi film can therefore be provided.

[0139]

In the above description, the polycide structure completely covered with the oxide film and the polycide structure partially covered with the oxide film are used for the word line and bit line in the memory cell area. Obviously, such polycide structures may be used singularly or in combination for both the word and bit lines.

Also in this embodiment, as the oxide film covering the gate electrode is made thicker, the structure becomes more resistant to separation of the silicide film. However, if the oxide film on the side wall of the gate electrode is formed by thermal oxidation, the oxide film cannot be made too thick because the MOS transistor characteristics may be deteriorated by the gate oxide bird's beak as described earlier. The oxide film on the upper surface of the gate electrode may be made thicker than that on the side wall of the gate electrode to provide the structure more resistant to separation without deteriorating the MOS transistor characteristics.

[3rd Embodiment]

The third embodiment will be described with reference to the schematic cross sectional views of Figs. 17 to 23. Similar to the first and second embodiments, Figs. 17 to 23 are schematic cross sectional views

showing a memory cell area taken along line A-A' of Fig. 1 and a typical wiring structure of a peripheral circuit area.

[0140]

The processes similar to the first embodiment are performed up to the process illustrated in Fig. 4(b). With these processes, polycide electrodes constituting the word lines and gate electrodes, nitride film regions 24, and the like are formed.

As shown in Fig. 17(a), a BPSG film 26 is grown to a thickness of 100 to 200 nm by CVD, and thereafter, heat treatment is performed at a temperature of 750 to 900 °C to planarize the surface of the BPSG film 26 through reflow.

[0141]

Etch-back or CMP may be used to further planarize the surface, similar to the first embodiment.

On the planarized BPSG film 26, a silicon nitride film 51 is grown by CVD to a thickness of 10 to 50 nm.

As shown in Fig. 17(b), a resist pattern is formed having an opening which exposes the source/drain regions of a MOS transistor in the memory cell area. By using this resist pattern as a mask, the nitride film 51, BPSG film 26, and oxide film 22 are sequentially etched to expose the substrate surface and form a contact window 27.

[0142]

Etching the nitride film 51 is performed by RIE

using CF_4 gas. When the surface of the BPSG film 26 is exposed, the gas is changed to mixed gas of C_4F_8 and CO to etch the BPSG film by RIE under the conditions of a higher etching selection ratio of oxide film relative to the nitride film so that the nitride film area 24 is not etched. The etching ratio to the nitride film is preferably 10 or higher.

[0143]

Also in this embodiment, the contact hole 27 is defined by a self alignment manner because of the nitride film spacer 24 and the polycide gate electrode is completely covered with the nitride film without exposing the oxide film. Therefore, the oxide film inside the spacer is not etched and removed even if there is misalignment of the opening of the resist pattern. Therefore, the gate electrode and contact electrode will not be electrically shorted as in the case of conventional techniques described with Figs. 35 to 37.

[0144]

Similar to the first embodiment, after the resist pattern is removed, by using the BPSG film 26 and nitride film region 24 as a mask, n-type impurity ions, phosphorus, are implanted at a dose of $3 \times 10^{13}cm^{-2}$ into the silicon substrate exposed in the contact window 27 to thereby form an n-type diffusion region 28.

Next, as shown in Fig. 18(a), a phosphorus doped silicon film is formed by CVD over the whole surface of

the substrate, and a plug 29 of the silicon film is left in the contact hole 27 by etch-back or CMP.

[0145]

The plug 29 of silicon may be formed by selective CVD without using etch-back or CMP.

A silicon oxide film 30 is then formed by CVD to a thickness of 30 to 100 nm.

As shown in Fig. 18(b), a resist pattern having an opening at a bit line connection area is formed. By using this resist pattern as a mask, the oxide film 30 is etched to form a contact window 31 exposing part of the upper surface of the silicon plug 29. Thereafter, the resist pattern is removed.

[0146]

Next, a phosphorus doped silicon film 32 of 30 nm thick, a WSi film 33 of 50 nm thick, and a silicon nitride film 34 of 80 nm thick are sequentially formed by CVD.

The lamination of these films is patterned to have a desired wiring pattern by well know photolithography. The polycide electrode of this lamination corresponds to a bit line (13 in Fig. 1) in the memory cell area, and to a wiring layer other than the bit line in the peripheral circuit area.

[0147]

Next, as shown in Fig. 19, a BPSG film 37 is grown to a thickness of 500 nm by CVD, and thereafter, heat treatment is performed at a temperature of 750 to 900 °C

to planarize the surface of the BPSG film 37 through reflow.

Etch-back or CMP may be used to further planarize the surface, or a combination of these processes may be used for planarization, similar to the first embodiment.

[0148]

Next, a resist pattern having an opening exposing the capacitor connection area is formed. By using this resist pattern as a mask, the BPSG Film 37 and oxide film 30 exposed in the opening are sequentially etched by RIE using, for example, mixed gas of C4F4 and CO to thereby form a contact window 38 exposing the upper surface of the silicon plug 29.

In this case, since the side surface of the polycide gate electrode is completely covered with the nitride film region 36, the oxide film is not etched and the bit line and storage electrode are not electrically shorted.

[0149]

In the first embodiment, as shown in Fig. 8, the BPSG film 26 is formed under the oxide film 30. Therefore, when the contact window 38 is formed by etching the BPSG film 35 and oxide film 28, there is a danger of etching the BPSG film 26 and forming a trench at the side of the plug 29 in the capacitor connection area.

Then, the shape and area of the storage electrode formed on the trench change and so the capacitance

changes. There is therefore a possibility that stable characteristics cannot be obtained.

[0150]

In contrast, in this embodiment, the nitride film 51 is formed under the oxide film 30. This nitride film 51 functions as an etching stopper at the connection area of the storage electrode when the BPSG film 37 and oxide film 30 are etched. Therefore, no trench is formed at the side of the plug 29 in the capacitor connection area. It is therefore possible to obtain stable capacitance and improve DRAM manufacture yield.

[0151]

Next, as shown in Fig. 20, after the resist pattern is removed, a phosphorous doped silicon film is formed by CVD to a thickness of 50 nm. The silicon film on the top flat surface is removed by polishing, for example CMP, or etch-back and a silicon film 39 is left at the side wall and bottom of the contact window 38.

Then, the BPSG film 37 is completely etched by using hydrofluoric acid containing etchant and by using the nitride film 51 as an etching stopper, to thereby form a hollow cylindrical storage electrode 39.

[0152]

In the first embodiment, as shown in Fig. 9, after the silicon film 39 is left only at the side wall and bottom of the contact window 38, the BPSG film is etched to a predetermined depth by hydrofluoric acid containing etchant as shown in Fig. 10 to thereby form the hollow

cylindrical storage electrode 39.

In this embodiment, by using the nitride film 51 as an etching stopper, the BPSG film 37 outside the silicon film 39 can be etched completely by hydrofluoric acid containing etchant. Therefore, variation of etching amounts of the BPSG film 37 is small so that the outer area of the cylinder type storage electrode can be maintained constant. It is therefore possible to manufacture stable DRAM cells with less variation of capacitance values.

[0153]

As shown in Fig. 21, a silicon nitride film is formed by CVD to a thickness of 40 nm, and thermally oxidized by 1 to 2 nm to thereby form a capacitor insulating film 39a on the surface of the storage electrode 39 (the capacitor insulating film is not shown).

Next, the phosphorous doped silicon film is formed by CVD to a thickness of 50 nm and patterned to form an opposing electrode 40 of the capacitor. At the patterning step, an unnecessary capacitor insulating film and silicon nitride film 51 are etched at the same time at the area outside of the pattern of the opposing electrode 40.

[0154]

In this state, although the silicon nitride film 51 may be left unetched, it is rather preferable to remove it from the following reason. If the silicon

nitride film is left at the peripheral circuit area, the succeeding process of forming a contact window for the diffusion region in the peripheral circuit area becomes complicated because both the oxide film and silicon nitride film should be etched. In addition, because of a difference of etching characteristics between silicon oxide film and silicon nitride film, the silicon nitride film in the contact window may form an overhang or eaves which may result in breakage of a metal wiring layer formed in the contact window.

[0155]

At the same time when the silicon nitride film 51 is etched, the silicon nitride film region 36 of the wiring layer in the peripheral circuit area is etched. It is therefore preferable that the silicon nitride film 34 on the WSi film 33 constituting the silicon nitride film region 36 is set thicker than the silicon nitride film 51.

[0156]

The succeeding processes are similar to the first embodiment, which processes form interlayer insulating film, contact windows and metal wiring layers to complete a DRAM.

As compared to the first embodiment, this embodiment uses the nitride film 51 serving as an etching stopper layer. The area of the storage electrode can be maintained constant during the processes of forming the storage electrode and its

contact window. Therefore, stable capacitance can be obtained and the DRAM manufacture yield can be improved.

[0157]

As another advantageous effect, a stable process of forming a contact window for the bit line can be expected. This will be clarified with reference to Figs. 22 and 23.

Figs. 22 and 23 are schematic cross sectional views of the memory cell area taken along line A-A' of Fig. 1A, illustrating a displaced contact window 31 shown in Fig. 18B. Fig. 22 shows no silicon nitride film 51 under the oxide film 30 and corresponds to the first embodiment, and Fig. 23 has the silicon nitride film 51 under the oxide film 30 and corresponds to the third embodiment.

[0158]

With the processes of the first embodiment, as shown in Fig. 22 if the contact window 31 is formed at a displaced area, the BPSG film 26 can be etched at the same time when the oxide film 30 is etched and a trench is formed at the side of the silicon plug 29.

This trench may break the bit line formed on the higher level layer or may be left as a void without being filled, or conversely the wiring layer left in the trench may electrically short adjacent plugs 29. There is therefore a danger of some adverse effects on the device.

[0159]

In contrast, in this embodiment, as shown in Fig. 23 even if the contact window 31 is formed at a displaced area, the nitride film 51 functions as the etching stopper. Therefore, there is no danger of etching the BPSG film 26 and no trench is formed at the side of the silicon plug 29, dispensing with the above adverse effects.

By positively using this nitride film stopper 49, it becomes possible to make the size of the contact widow 31 larger than the silicon plug 29 so that a margin of a process of forming a contact window can be increased.

[4th Embodiment]

The fourth embodiment will be described with reference to the schematic cross sectional views of Figs. 24 to 28. Similar to the first and second embodiments, Figs. 24 to 28 are schematic cross sectional views showing a memory cell area taken along line A-A' of Fig. 1 and a typical wiring structure of a peripheral circuit area.

[0160]

The processes similar to the first embodiment are performed up to the process illustrated in Fig. 6(b). With these processes, the polycide electrodes and silicon nitride film regions 36, and the like are formed above the word lines and MOS transistors of the peripheral circuit area, to serve as the bit lines and wiring layers in the peripheral circuit area.

As shown in Fig. 24, a BPSG film 52 is grown by CVD over the whole surface of the substrate, and thereafter, heat treatment is performed at a temperature of 750 to 900 °C to planarize the surface of the BPSG film 52 through reflow.

[0161]

Etch-back or CMP may be used to further planarize the surface, or the combination of these processes may be used.

Next, a silicon nitride film 53 and a BPSG film 54 are sequentially grown by CVD.

The total thickness of the BPSG films 52 and 54 is set to 500 nm, and that of the silicon nitride film 53 is set to 10 to 50 nm.

[0162]

The thickness of the BPSG film 52 is so set that it can be planarized. The thickness of the BPSG film 54 defines the area of the outer surface of the cylinder type storage electrode directly related to the capacitance. Therefore, the thickness of the BPSG film 54 is determined from a necessary capacitance. The thickness ratio and total thickness of the BPSG films 50 and 52 are therefore set in accordance with the above two conditions.

As shown in Fig. 25, a resist pattern is formed having an opening which exposes the capacitor connection area. By using this resist pattern as a mask, the BPSG film 54 exposed in the opening of the resist pattern is

etched by RIE using mixed gas of C_4F_8 and CO, the nitride film 53 is next etched by RIE using CF4 gas, and then the BPSG film 52 and oxide film 30 are sequentially etched by RIE using mixed gas of C_4F_8 and CO, to thereby form a contact window 38 exposing the upper surface of the silicon plug 29.

[0163]

As shown in Fig. 26, after the resist film is removed, a phosphorus doped silicon film is formed by CVD to a thickness of 50 nm over the whole surface of the substrate, and by using etch-back or CMP, a silicon film 39 is left only at the bottom and side wall of he contact window 38.

As shown in Fig. 27, the BPSG film 54 outside the silicon film 39 is completely etched by using hydrofluoric acid containing etchant. Since the nitride film 53 functions as the etching stopper, only the BPSG film 54 can be completely removed. With this process, a hollow cylindrical storage electrode 39 can be formed.

[0164]

Also in this embodiment, similar to the third embodiment, the BPSG film 54 outside the cylinder type storage electrode 39 can be completely removed. Therefore, the outer area of the cylinder type storage electrode can be maintained constant. It is therefore possible to manufacture stable DRAM cells with less variation of capacitance values.

As shown in Fig. 28, a silicon nitride film is

formed by CVD to a thickness of 40 nm, and thermally oxidized by 1 to 2 nm to thereby form a capacitor insulating film on the surface of the storage electrode 39a (the capacitor insulating film is not shown).

Next, the phosphorous doped silicon film is formed by CVD to a thickness of 50 nm and patterned to form an opposing electrode 40 of the capacitor. Following the patterning of the electrode 40, an unnecessary capacitor insulating film and silicon nitride film 53 are etched at the area outside of the pattern of the opposing electrode 40.

[0165]

In this case, similar to the embodiment of the fourth DRAM, although the silicon nitride film 53 may be left unetched, it is rather preferable to remove it in the peripheral circuit area from the following reason, similar to the third embodiment. If the silicon nitride film is left at the peripheral circuit area, the succeeding process of forming a contact window for the diffusion region in the peripheral circuit area becomes complicated because both the oxide film and silicon nitride film should be etched. In addition, because of a difference of etching characteristics between silicon oxide and silicon nitride, the silicon nitride film in the contact window may form an overhang which may result in breakage of a metal wiring layer formed in the contact window.

[0166]

The succeeding processes are similar to the first embodiment, which processes form interlayer insulating layer, contact windows and metal wiring layers to complete a DRAM.

In this embodiment, only the BPSG film 52 outside of the cylinder type storage electrode 37 can be completely removed. It is therefore possible to manufacture stable DRAM cells with less variation of capacitance values.

[0167]

As shown in Fig. 11 of the first embodiment, after the capacitor opposing electrode 38 is formed, planarization is performed by using the insulating film. In this fifth embodiment, it is obvious that planarization at the later process becomes easier because a difference of height between the memory cell area and peripheral circuit area is reduced.

In this embodiment, therefore, process design can be carried out by considering both the effects that stable capacitance can be obtained and that planarization becomes easy because of a small difference of height between the memory cell area and peripheral circuit area. It is therefore possible to manufacture DRAMs of stable characteristics.

[0168]

The nitride film 53 is etched at the same time when the opposing electrode 38 is patterned. Therefore, similar to the third embodiment, problems to be caused

by the silicon nitride film in the peripheral circuit area can be eliminated.

As different from the third embodiment, the BPSG film 52 exists under the silicon nitride film 53 so that the BPSG film 52 can be etched by using the silicon nitride film 53 as the etching stopper and there is no fear of etching the silicon nitride film region 34 of the wiring layer in the peripheral circuit area corresponding to the bit line in the memory cell area.

[5th Embodiment]

The fifth embodiment will be described with reference to Figs. 29 and 30. This embodiment pertains to a method of forming the contact windows 42 to 45 for the first metal wiring layer of the first embodiment shown in Fig. 13.

[0169]

Fig. 29 shows the contact windows 42 to 45 formed by the embodiment method, after the opposing electrode 40 is formed and the BPSG film is planarized by the first embodiment method.

First, a first step of forming the contact windows 42 to 45 is performed to etch the BPSG film 41 at a sufficiently large etching ratio of the BPSG film 41 to the nitride film. This etching may use mixed gas of C_4F_8 and CO used for forming the nitride film SAC structure.

[0170]

The first etching step continues until the surface of the lowermost diffusion region 25 is exposed.

Although the opposing electrode 40 at the uppermost layer is etched and removed, the etching stops at this level and the lower BPSG film 26 is not etched because the nitride film 51 exists under the opposing electrode. The etching of the contact windows 43 and 44 also stops at the nitride film regions 36 and 25.

[0171]

Next, a second etching step etches the silicon nitride film at a large etching ratio of the silicon nitride film relative to etching of an oxide film such as BPSG, by using, for example, mixed gas of CHF_3 and O2. With this process, the nitride film regions 36 and 25 at the bottoms of the contact windows 43 and 44 can be removed.

When the nitride film is etched, the nitride film 51 under the opposing electrode 40 is also etched. However, etching stops at the underlying BPSG film 26 so that the opposing electrode 40 and the lower wiring layer are not electrically shorted at the contact window 42. This contact window structure poses no practical problem because the first metal wiring layer formed in the contact window is electrically connected to the opposing electrode 40 at its side wall.

[0172]

Fig. 30 shows the contact windows 42 to 45 formed by the embodiment method after the opposing electrode 40 is formed and the BPSG film is planarized by the fourth embodiment method.

Since the DRAM shown in Fig. 30 has the nitride film 53 and BPSG film 52 under the opposing electrode 40 similar to the DRAM shown in Fig. 29, the above-described two etching steps can be used. Therefore, the contact windows 42 to 45 can be formed by a single photolithography process without a problem of short circuit to the underlying wiring layer.

[0173]

With this embodiment, contact windows can be formed by a single photolithography process even for the structure having different contact window depths.

If the nitride film is not formed at the bottoms of the contact windows 41 and 42 and the first step can expose the surfaces of the wiring layer and the gate electrode, the second step of etching the nitride film is not necessary.

[0174]

The method of forming a contact window of this embodiment is not limited to only to the above. For example, it is obvious that the same advantages can be obtained by providing a nitride film under a higher level wiring layer among a plurality of wiring layers and using the nitride film as the etching stopper.

However, if this embodiment itself is used without modification, in addition to the advantages specific to this embodiment, the advantages of the third and fourth embodiments can be obtained.

[6th Embodiment]

The sixth embodiment will be described with reference to the schematic cross sectional view of Fig. 31.

[0175]

In the first embodiment shown in Fig. 5(a), the BPSG film 24 is planarized by reflow, etch-back, or CMP.

In this embodiment, as shown in Fig. 31, the BPSG film 26 formed on the gate electrode and word line is planarized by CMP by using the silicon nitride film region 24 as its stopper layer.

[0176]

A distance from the substrate to the silicon nitride film region 24 covering the polycide electrode of the gate electrode on the active region is different from that of the wiring layer on the field oxide film 17. In this embodiment, only the higher nitride film spacer is used as the stopper layer and the BPSG film 26 is left on the lower nitride film spacer.

[0177]

For example, if silica containing material is used as abrasive material, the BPSG film can be abraded or polished at a high abrasion or polishing selection ratio of the BPSG film to the silicon nitride film.

This stopper layer not only planarizes the BPSG film 26 but also reduces a variation of film thickness.

[0178]

If there is a variation of film thickness of the planarized BPSG film, the etching amount at the later

contact window forming process is scattered. In order to obtain a reliable contact, it is necessary to completely remove the BPSG film in the contact window so that an over-etch amount of the BPSG film is required to be made large.

This over-etch reduces the thickness of the nitride film spacer of the nitride film spacer SAC structure, increasing a danger of a short circuit between the polycide electrode and upper wiring layer. Therefore, the stable film thickness of the BPSG film is particularly important.

[0179]

In this embodiment, the nitride film region 24 itself which is necessary for the nitride spacer SAC structure is used without forming an additional stopper layer. The number of processes does not therefore increases.

After the BPSG film is planarized by CMP, another BPSG film may be formed to thicken the interlayer insulating film and reduce parasitic capacitance. As described with the embodiment of the fourth DRAM, the contact window forming process may be performed after the silicon nitride film is formed.

[0180]

The thickness of the BPSG film 26 influences the parasitic capacitance of the bit line formed at the upper layer. If the variation of film thickness is reduced as in this embodiment, the variation of bit line

capacitance can be reduced and the operation stability of DRAM can be improved.

Also in this embodiment, only the nitride spacer of the word line and wiring layer on the field insulating film is used as the stopper layer, and the nitride film spacer of the gate electrode on the active region is not used as the stopper layer.

[0181]

Therefore, while the BPSG film is abraded by CMP, the nitride film spacer at the active region will not be abraded and the film thickness is not reduced.

With the nitride film SAC, a contact window is formed in a self alignment manner by using the nitride film spacer as a mask. The contact window is formed not over the field insulating film but over the diffusion region in the active region. Therefore, the nitride film spacer SAC process can use as a mask the nitride film whose thickness is not reduced during planarization by CMP.

In this embodiment, therefore, while planarization by CMP can be performed with high controllability by using the stopper layer, the polycide electrode and upper wiring layer can be avoided from being electrically shorted via the contact hole formed by the nitride film spacer SAC process.

[0182]

With this embodiment, product yield and operation stability can be improved without increasing the number

of processes.

[7th Embodiment]

The seventh embodiment will be described with reference to the schematic cross sectional view of Fig. 32.

In this embodiment, the techniques of the sixth embodiment is utilized for the process of planarizing the surface of the BPSG film on the conductive layer of bit lines.

[0183]

In the first embodiment shown in Fig. 7, the BPSG film 37 is planarized by reflow, etch-back, or CMP.

In this embodiment, as shown in Fig. 32, the BPSG film 37 formed on the bit line is planarized by CMP by using the silicon nitride film region 36 as its stopper layer.

[0184]

For example, if silica containing material is used as abrasive material, the BPSG film can be abraded at a high abrasion selection ratio of the BPSG film to the silicon nitride film, similar to the sixth embodiment.

This stopper layer not only planarizes the BPSG film 37 but also reduces a variation of film thickness.

[0185]

If there is a variation of film thickness of the planarized BPSG film, the etching amount at the later contact window forming process is scattered. Therefore, if the thickness of the nitride film spacer of the

nitride film spacer SAC structure is reduced, a danger of a short circuit between the polycide electrode and upper wiring layer increases so that the stable film thickness of the BPSG film is particularly important, as in the case of the sixth embodiment.

Also in this embodiment, the nitride film region 36 itself which is necessary for the nitride spacer SAC structure is used without forming an additional stopper layer. The number of processes does not therefore increases.

[0186]

Since the thickness of the BPSG film 37 influences the area of the storage electrode and hence the capacitance, after the CMP planarization another BPSG film may be formed to set a desired thickness and obtain a desired capacitance. Similar to the embodiment of the fifth DRAM, two layers of BPSG films with a nitride film being interposed may be used.

[8th Embodiment]

The eighth embodiment will be described with reference to the schematic cross sectional view of Fig. 33.

[0187]

In the first embodiment shown in Fig. 5(a), the n-type diffusion region 26is formed in order to reduce junction leak.

In this embodiment, as shown in Fig. 33 the n-type diffusion region 28 is formed only in the source/drain

region on the side of a capacitor of the memory cell. After the source/drain region to which the bit line is connected is covered with a resist pattern 55, n-type impurity ions, phosphorous, are implanted at a dose of 3 x $10^{13}cm^{-2}$ into the silicon substrate exposed in the contact holes 27 by using the BPSG film 26 and nitride film regions 24 as a mask.

[0188]

The n-type diffusion region 28 can suppress junction leak as described with the embodiment of the first DRAM. However, this ion implantation deepens the junction of the source/drain regions. Therefore, the short channel effects of transistors may be adversely affected or leak current between elements may increase.

The diffusion region which stores small electric charges on the capacitor side is required to reduce junction leak, whereas junction leak is not severe for the diffusion region connected to the bit line.

[0189]

In this embodiment, therefore, ions are implanted only into the diffusion region connected to the capacitor so that one of the source/drain regions of a MOS transistor can be made to have a shallow junction and the short channel effects of transistors and leak current between elements can be prevented from being adversely affected.

The present invention has been described in connection with the first to eighth embodiments. The

invention is not limited only to the above embodiments. It is obvious that the invention is applicable to processes having the same technical concept as the above-described processes.

[0190]

In the above description, WSi is used as the polycide electrode. Other silicide materials such as MoSi and TiSi may also be used. In addition to silicide, metals and metal compounds may be used, including tungsten (W), molybdenum (Mo), titanium nitride (TiN), and titanium tungsten (TiW). Since an oxide film is difficult to be formed on metal or metal compound by thermal oxidation, an oxide film may be formed by CVD or the like.

[0191]

In the above description, a silicon oxide film is used as the insulating film formed between the gate electrode and nitride film. Other insulating films may also be used if they can relax strains in the silicon nitride film. If a silicon oxynitride (SiON) film is used, it can be used also as an antireflection film on the silicide film so that the number of processes can be effectively shortened.

Although BPSG is used as an interlayer insulating film, other materials such as PSG and a silicon oxide film may also be used.

[0192]

Although isotropic etching of wet etching and

anisotropic etching of RIE are used as the etching method, other etching such as isotropic plasma etching and ECR etching may be selectively used depending upon processes.

Although a phosphorous doped silicon film is used as the plug formed in the contact window, a silicon film doped with p-type impurities such as boron may be used if the plug is formed on the p-type diffusion region or p-type silicon layer. The material of the plug is not limited only to the silicon film, but metals and metal compounds such as W and TiW or metal silicide may also be used.

[0193]

Although the oxidized nitride film is used as the capacitor insulating film, high dielectric constant films and ferroelectric films such as a tantalum oxide (Ta_2O_5) film and a PZT film may also be used. In this case, metal is used as the storage electrode and/or the opposing electrode so that a capacitance reduction by natural oxidation of the electrode can be prevented and reaction between the capacitor insulating film and silicon film can be avoided.

[0194]

As the silicon film, polysilicon or amorphous silicon may be used. Impurity doping may be performed at the same time when the film is grown, or diffusion or ion implantation may be performed after the film is grown.

In the above embodiments, although a method of forming a cylinder type capacitor is used, obviously the invention is applicable to other capacitor structures such as a stack type and a fin type.

[0195]

[Effect of Invention]

According to the invention, nitride film spacer SAC is possible without degrading the reliability of MOS transistors while preventing a peel-off of a metal silicide film constituting a gate electrode.

The invention is suitable for making fine DRAM, increasing manufacture margins, and reducing manufacture processes.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

Diagrams illustrating the invention.

[Fig. 2]

A schematic plan view showing a memory cell area of the invention.

[Fig. 3]

Schematic cross sectional views (part 1) illustrating a first embodiment of the invention.

[Fig. 4]

Schematic cross sectional views (part 2) illustrating the first embodiment of the invention.

[Fig. 5]

Schematic cross sectional views (part 3) illustrating the first embodiment of the invention.

[Fig. 6]

Schematic cross sectional views (part 4) illustrating a first embodiment of the invention.

[Fig. 7]

A schematic cross sectional view (part 5) illustrating the first embodiment of the invention.

[Fig. 8]

A schematic cross sectional view (part 6) illustrating the first embodiment of the invention.

[Fig. 9]

A schematic cross sectional view (part 7) illustrating the first embodiment of the invention.

[Fig. 10]

A schematic cross sectional view (part 8) illustrating the first embodiment of the invention.

[Fig. 11]

A schematic cross sectional view (part 9) illustrating the first embodiment of the invention.

[Fig. 12]

A schematic cross sectional view (part 10) illustrating a first embodiment of the invention.

[Fig. 13]

A schematic cross sectional view (part 11) illustrating the first embodiment of the invention.

[Fig. 14]

A schematic cross sectional view (part 12) illustrating the first embodiment of the invention.

[Fig. 15]

Schematic cross sectional views (part 1) illustrating a second embodiment of the invention.

[Fig. 16]

Schematic cross sectional views (part 2) illustrating the second embodiment of the invention.

[Fig. 17]

Schematic cross sectional views (part 1) illustrating a third embodiment of the invention.

[Fig. 18]

Schematic cross sectional views (part 2) illustrating the third embodiment of the invention.

[Fig. 19]

A schematic cross sectional view (part 3) illustrating the third embodiment of the invention.

[Fig. 20]

A schematic cross sectional view (part 4) illustrating the third embodiment of the invention.

[Fig. 21]

A schematic cross sectional view (part 5) illustrating the third embodiment of the invention.

[Fig. 22]

A schematic cross sectional view (part 1) illustrating the effects of the third embodiment of the invention.

[Fig. 23]

A schematic cross sectional view (part 2) illustrating the effects of the third embodiment of the invention.

[Fig. 24]

A schematic cross sectional view (part 1) illustrating a fourth embodiment of the invention.

[Fig. 25]

A schematic cross sectional view (part 2) illustrating the fourth embodiment of the invention.

[Fig. 26]

A schematic cross sectional view (part 3) illustrating the fourth embodiment of the invention.

[Fig. 27]

A schematic cross sectional view (part 4) illustrating the fourth embodiment of the invention.

[Fig. 28]

A schematic cross sectional view (part 5) illustrating the fourth embodiment of the invention.

[Fig. 29]

A schematic cross sectional view (part 1) illustrating a fifth embodiment of the invention.

[Fig. 30]

A schematic cross sectional view (part 2) illustrating the fifth embodiment of the invention.

[Fig. 31]

A schematic cross sectional view illustrating a sixth embodiment of the invention.

[Fig. 32]

A schematic cross sectional view illustrating a seventh embodiment of the invention.

[Fig. 33]

A schematic cross sectional view illustrating an eighth embodiment of the invention.

[Fig. 34]

Schematic cross sectional views (part 1) illustrating nitride film spacer SAC.

[Fig. 35]

Schematic cross sectional views (part 2) illustrating nitride film spacer SAC.

[Fig. 36]

Schematic cross sectional views (part 1) illustrating problems associated with conventional techniques.

[Fig. 37]

A schematic cross sectional view (part 2) illustrating problems associated with conventional techniques.

[Description of Reference Symbols]

4, 19, 114... silicon film, 5, 20, 15... silicide film, 6, 22... silicon oxide film, 7, 23, 116... n^--type impurity diffusion layer, 8, 24, 117... silicon nitrate film region, 9, 26, 118... BPSG film, 10, 27, 119... contact window, 25... n^+-type impurity diffusion layer, 28... n-type impurity diffusion layer, 31... contact window, 32... silicon film, 33... silicide film, 34... silicon nitrate film, 35... silicon oxide film, 36... silicon nitrate film region, 38... contact window, 39... cylinder type storage electrode, 40... capacitor opposing electrode, 41... BPSG film, 42, 43, 44, 45...

contact window, 48, 50... silicon oxide film region, 51, 53... silicon nitrate film, 52, 54... BPSG film, 123... silicon oxide film, 124... silicon nitrate film

[NAME OF DOCUMENT] Abstract

[ABSTRACT]

[OBJECT]

A semiconductor device and its manufacture method are provided which can realize high integrated DRAMs of 256 M or larger without degrading reliability and stability.

[CONSTRUCTION]

A semiconductor device and its manufacture method wherein the semiconductor substrate has first and second insulating films, the first insulating film being an insulating film other than a silicon nitride film formed on a side wall of a conductive pattern including at least one layer of metal or metal silicide, and the second insulating film being a silicon nitride film formed to cover the first insulating film formed on an upper surface and side wall of the conductive pattern. The first insulating film may be formed to cover the upper surface and side wall of the conductive pattern.

[Selected Figure] Fig. 1

FIG. 1

ILLUSTRATION OF THE INVENTION

FIG. 2

PLAN VIEW OF EMBODIMENT OF THE INVENTION

FIG. 3

SCHEMATIC CROSS SECTIONAL VIEW OF PROCESS OF 1ST EMBODIMENT (PART 1)

FIG. 15

SCHEMATIC CROSS SECTIONAL VIEW OF PROCESS OF 2ND EMBODIMENT (PART 1)

FIG. 17

SCHEMATIC CROSS SECTIONAL VIEW OF PROCESS OF 3RD EMBODIMENT (PART 1)

FIG. 24

SCHEMATIC CROSS SECTIONAL VIEW OF PROCESS OF 4TH EMBODIMENT (PART 1)

FIG. 29

SCHEMATIC CROSS SECTIONAL VIEW OF PROCESS OF 5TH EMBODIMENT (PART 1)

FIG. 31

SCHEMATIC CROSS SECTIONAL VIEW OF PROCESS OF 6TH EMBODIMENT

FIG. 32

SCHEMATIC CROSS SECTIONAL VIEW OF PROCESS OF 7TH EMBODIMENT

FIG. 33

SCHEMATIC CROSS SECTIONAL VIEW OF PROCESS OF 8TH EMBODIMENT

FIG. 34

SCHEMATIC CROSS SECTIONAL VIEW OF NITRIDE FILM SPACER SAC PROCESS (PART 1)

FIG. 36

DIAGRAM ILLUSTRATING PROBLEMS OF CONVENTIONAL EXAMPLE (PART 1)